ASTRO® Digital XTL™ 5000

VHF
UHF Range 1 and 2
700–800 MHz
Mobile Radio

Detailed Service Manual

MOTOROLA

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ASTRO® Digital XTL™ 5000

VHF/UHF Range 1/UHF Range 2/
700–800 MHz
Mobile Radio

Detailed Service Manual

Motorola, Inc.
8000 West Sunrise Boulevard
Fort Lauderdale, Florida 33322

6881096C74-B

Foreword

The information contained in this manual relates to all ASTRO® Digital XTL™ 5000 VHF/UHF Range 1/UHF Range 2/700–800 MHz mobile radios equipped with W3, W4, W5, W7, or W9 control heads, unless otherwise specified. This manual provides sufficient information to enable qualified service technicians to troubleshoot and repair XTL 5000 radios to the component level.

For details on radio operation or basic troubleshooting, refer to the applicable manuals available separately. A list of related publications is provided in the section, “Related Publications,” on page xxii.

Product Safety and RF Exposure Compliance

Before using this product, read the operating instructions for safe usage contained in the Product Safety and RF Exposure booklet enclosed with your radio.

ATTENTION!

This radio is restricted to occupational use only to satisfy FCC RF energy exposure requirements. Before using this product, read the RF energy awareness information and operating instructions in the Product Safety and RF Exposure booklet enclosed with your radio (Motorola Publication part number 6881095C99) to ensure compliance with RF energy exposure limits.

For a list of Motorola-approved antennas, batteries, and other accessories, visit the following web site which lists approved accessories: http://www.motorola.com/cgiss/index.shtml.

Manual Revisions

Changes which occur after this manual is printed are described in FMRs (Florida Manual Revisions). These FMRs provide complete replacement pages for all added, changed, and deleted items, including pertinent parts list data, schematics, and component layout diagrams. To obtain FMRs, contact the Radio Products and Services Division (refer to “Appendix B Replacement Parts Ordering").

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Document History

The following major changes have been implemented in this manual since the previous edition:

Edition	Description	Date
6881096C74-B	Added VHF High Power and UHF R1 High Power models.	May, 2005

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Related Publications

Commercial Warranty

Limited Warranty

MOTOROLA COMMUNICATION PRODUCTS

I. What This Warranty Covers And For How Long

MOTOROLA INC. (“MOTOROLA”) warrants the MOTOROLA manufactured Communication Products listed below (“Product”) against defects in material and workmanship under normal use and service for a period of time from the date of purchase as scheduled below:

ASTRO Digital XTL 5000 Mobile Radio Units	One (1) Year
Product Accessories	One (1) Year

Motorola, at its option, will at no charge either repair the Product (with new or reconditioned parts), replace it (with a new or reconditioned Product), or refund the purchase price of the Product during the warranty period provided it is returned in accordance with the terms of this warranty. Replaced parts or boards are warranted for the balance of the original applicable warranty period. All replaced parts of Product shall become the property of MOTOROLA.

This express limited warranty is extended by MOTOROLA to the original end user purchaser only and is not assignable or transferable to any other party. This is the complete warranty for the Product manufactured by MOTOROLA. MOTOROLA assumes no obligations or liability for additions or modifications to this warranty unless made in writing and signed by an officer of MOTOROLA. Unless made in a separate agreement between MOTOROLA and the original end user purchaser, MOTOROLA does not warrant the installation, maintenance or service of the Product.

MOTOROLA cannot be responsible in any way for any ancillary equipment not furnished by MOTOROLA which is attached to or used in connection with the Product, or for operation of the Product with any ancillary equipment, and all such equipment is expressly excluded from this warranty. Because each system which may use the Product is unique, MOTOROLA disclaims liability for range, coverage, or operation of the system as a whole under this warranty.

II. General Provisions

This warranty sets forth the full extent of MOTOROLA's responsibilities regarding the Product. Repair, replacement or refund of the purchase price, at MOTOROLA's option, is the exclusive remedy. THIS WARRANTY IS GIVEN IN LIEU OF ALL OTHER EXPRESS WARRANTIES. IMPLIED WARRANTIES, INCLUDING WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED TO THE DURATION OF THIS LIMITED WARRANTY. IN NO EVENT SHALL MOTOROLA BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, FOR ANY LOSS OF USE, LOSS OF TIME, INCONVENIENCE, COMMERCIAL LOSS, LOST PROFITS OR SAVINGS OR OTHER INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

III. State Law Rights

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES OR LIMITATION ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATION OR EXCLUSIONS MAY NOT APPLY.

This warranty gives specific legal rights, and there may be other rights which may vary from state to state.

IV. How To Get Warranty Service

You must provide proof of purchase (bearing the date of purchase and Product item serial number) in order to receive warranty service and, also, deliver or send the Product item, transportation and insurance prepaid, to an authorized warranty service location. Warranty service will be provided by Motorola through one of its authorized warranty service locations. If you first contact the company which sold you the Product, it can facilitate your obtaining warranty service. You can also call Motorola at 1-888-567-7347 US/Canada.

V. What This Warranty Does Not Cover

A. Defects or damage resulting from use of the Product in other than its normal and customary manner.

B. Defects or damage from misuse, accident, water, or neglect.

C. Defects or damage from improper testing, operation, maintenance, installation, alteration, modification, or adjustment.

D. Breakage or damage to antennas unless caused directly by defects in material workmanship.

E. A Product subjected to unauthorized Product modifications, disassemblies or repairs (including, without limitation, the addition to the Product of non-Motorola supplied equipment) which adversely affect performance of the Product or interfere with Motorola's normal warranty inspection and testing of the Product to verify any warranty claim.

F. Product which has had the serial number removed or made illegible.

G. Rechargeable batteries if:

- any of the seals on the battery enclosure of cells are broken or show evidence of tampering.
- the damage or defect is caused by charging or using the battery in equipment or service other than the Product for which it is specified.

H. Freight costs to the repair depot.

I. A Product which, due to illegal or unauthorized alteration of the software/firmware in the Product, does not function in accordance with MOTOROLA's published specifications or the FCC type acceptance labeling in effect for the Product at the time the Product was initially distributed from MOTOROLA.

J. Scratches or other cosmetic damage to Product surfaces that does not affect the operation of the Product.

K. Normal and customary wear and tear.

VI. Patent And Software Provisions

MOTOROLA will defend, at its own expense, any suit brought against the end user purchaser to the extent that it is based on a claim that the Product or parts infringe a United States patent, and MOTOROLA will pay those costs and damages finally awarded against the end user purchaser in any such suit which are attributable to any such claim, but such defense and payments are conditioned on the following:

A. that MOTOROLA will be notified promptly in writing by such purchaser of any notice of such claim;

B. that MOTOROLA will have sole control of the defense of such suit and all negotiations for its settlement or compromise; and

C. should the Product or parts become, or in MOTOROLA's opinion be likely to become, the subject of a claim of infringement of a United States patent, that such purchaser will permit MOTOROLA, at its option and expense, either to procure for such purchaser the right to continue using the Product or parts or to replace or modify the same so that it becomes noninfringing or to grant such purchaser a credit for the Product or parts as depreciated and accept its return. The depreciation will be an equal amount per year over the lifetime of the Product or parts as established by MOTOROLA.

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VII. Governing Law

This Warranty is governed by the laws of the State of Illinois, USA.

Notes

Model Numbering, Charts, and Specifications

Mobile Radio Model Numbering Scheme

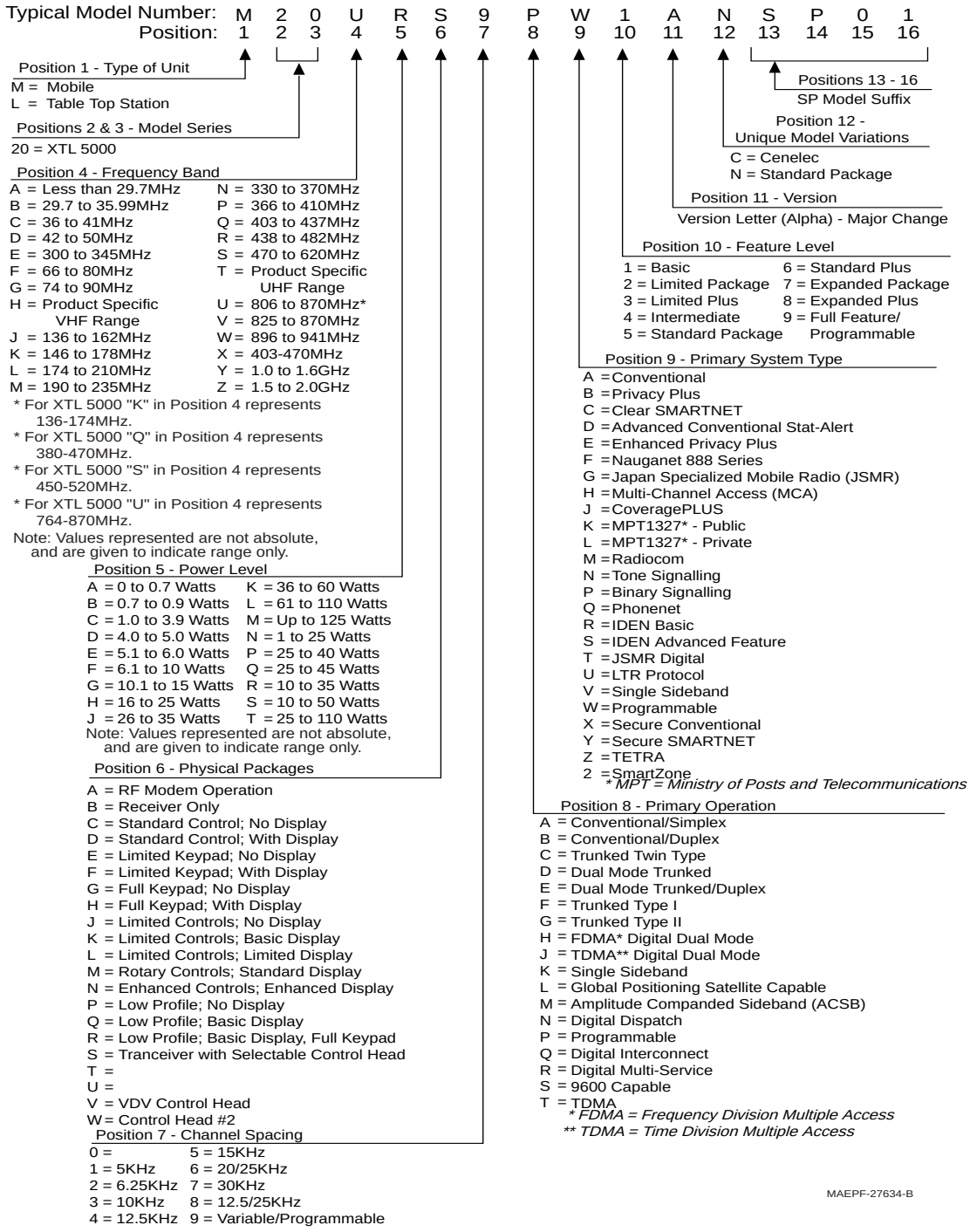

Figure 1. Mobile Radio Model Numbering Scheme

ASTRO XTL 5000 Motorcycle VHF 10-50 Watt Model Chart

M20KSS9PW1AN 136–174 MHz

Option												Description
G67AD												ADD: Remote Control Microphone W4, W5, W7
	G67AF											ADD: Remote Mount No Control Head Needed
		G82AA										ADD: Motorcycle W4 Control Head
			G83AA									ADD: Motorcycle W5 Control Head
				G84AA								ADD: Motorcycle W7 Control Head
					G159AC							ADD: Encryption UCM Hdw 3-Day Key Ret
						G159AD						ADD: Encryption UCM Hdw 30-Sec Key Ret
							W22AT					ADD: Hand Microphone (Motorcycle WP Mic)
								W15AG				ADD: Black Weather Resistant Enclosure
									G151AA			ADD: White Weather Resistant Enclosure
										B18CM		ADD: Auxiliary Speaker Spec Motorcycle
											Item No.	Description
X	X	X									HLN6863_	Accessory Connector
X											HUF4022_	VHF 136-174 MHz Main Board
	X	X									HLN6861_	Hardware Standard Install
	X										HLN6842_	Motorcycle Hardware 800 15 w w/W90
	X	X									HLN6884_	Motorcycle Interconnect Board
	X	X									HKN4191_	Mobile Power Cable
	X	X									HKN6062_	Motorcycle Control Head Cable 8'
	X	X									HLN6865_	Remote Mount Control Head Interconnect
		X									HLN6125_	Hardware Housing Front Remote
			X								PMLN4019_	W4 Motorcycle Control Head
				X	X						HLN6105_	Spare Button Kit
				X	X						HLN6688_	Spare Button Kit
						X					HLN6876_	Secure Interface Board 3-Day Key Retention
							X				HLN6877_	Secure Interface Board 30-Sec Key Retention
								X			HMN1079_	Motorcycle Palm Microphone
										X	HSN6003_	Motorcycle Water Resistant Speaker
									X	X	HKN6032_	Motorcycle Power Cable
										X	HLN1445_	White Motorcycle Enclosure and Hardware
									X		HLN1446_	Black Motorcycle Enclosure and Hardware

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 VHF 10-50 Watt Model Chart

M20KSS9PW1AN 136–174 MHz

Option	Description
G66AA	ADD: Dash Mount W4, W5, W7
G66AB	ADD: Dash Mount W3
G66AC	ADD: Dash Mount No Control Head Needed
G67AA	ADD: Remote Mount W4, W5, W7
G67AB	ADD: Remote Mount W9
G67AC	ADD: Remote Mount W3
G67AE	ADD: Remote Mount No Control Head
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W382AG	ALT: Control Station Palm Microphone
W665BE	ADD: Control Station Operation
G91AA	ADD: Control Station Power Supply

G66AA	G66AB	G66AC	G67AA	G67AB	G67AC	G67AE	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W382AG	W665BE	G91AA	Item No.	Description
X																	HUD4022_	VHF 136-174 MHz Main Board
	X	X	X	X	X	X	X										HLN6861_	Installation Hardware
	X	X	X	X	X	X	X										HLN6863_	Accessory Connector Plug
	X	X	X														HKN4191_	Mobile Power Cable
		X				X											HLN6885_	Handheld CH Interconnect Board
				X	X		X										HLN6883_	Remote Interconnect Board
				X													HLN6813_	Control Head Trunnion Kit
				X													HLN6432_	Back Housing Kit
				X	X	X	X										HKN4192_	Mobile Power Cable 20 ft.
				X	X	X											HKN4356_	Standard 17 ft Control Head Remote Cable
				X	X	X											HKN6096_	Handheld Control Head Y Cable
					X												HLN4921_	Trunnion
							X										HMN4044_	Handheld Control Head
								X	X	X							HLN6105_	Spare Button Kit
								X	X	X							HLN6688_	Spare Button Kit
									X	X							HLN6396_	CH DEK Compatible
											X						HCN1078_	W9 Control Head
														X			HMN1050_	Control Station Microphone
												X					HLN6876_	Secure Interface Board 3-Day Key Retention
													X				HLN6877_	Secure Interface Board 30-Sec Key Retention
															X		HLN6042_	Base Tray
															X		HLN6047_	BDW Installation Base Tray
																X	HPN4001_	Control Station Power Supply

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 VHF 10-50 Watt Model Chart (cont.)

M20KSS9PW1AN 136–174 MHz

Option	Description
W22AR	ADD: W9 Palm Microphone
W22AS	ADD: Hand Microphone
W109CS	ALT: Microphone Handset with Hangup Cup
B18CL	ADD: Auxiliary Spkr Spectra 5 Watt
W432AE	ENH: 10-Watt Audio (Standard on High Power)
G296AA	ADD: Antenna, 1/4 Wave Whip Roof Top VHF (136-144 MHz)
G297AA	ADD: Antenna, 1/4 Wave Roof Top VHF (144-150.8 MHz)
G299AA	ADD: Antenna, 1/4 Wave Roof Top VHF (150.8-162 MHz)
G300AA	ADD: Antenna, VHF (162-174 MHz, 3.4 MHz Bandwidth), 3 dB Roof Top
G301AA	ADD: Antenna, VHF (136-174 MHz, 3.4 MHz Bandwidth) 3 dB Roof Top

W22AR	W22AS	W109CS	B18CL	W432AE	G296AA	G297AA	G299AA	G300AA	G301AA	Item No.	Description
X										HMN1061_	W9 Palm Microphone
	X									HMN1080_	Standard Palm Microphone W4, W5, W7
		X								HLN1220_	Microphone Handset with Hangup Clip
			X							HSN4018_	Speaker 5 Watt
				X						HSN6001_	Speaker 10 Watt
					X					HAD4006_	Antenna,VHF (136-144 MHz) 1/4 Wave Roof Top
						X				HAD4007_	Antenna,VHF (144-150.8 MHz) 1/4 Wave Roof Top
							X			HAD4008_	Antenna,VHF (150.8-162 MHz) 1/4 Wave Roof Top
								X		HAD4009_	Antenna,VHF (162-174 MHz) 1/4 Wave Roof Top
									X	RAD4010ARB	Antenna,VHF (136-174 MHz, 3.4 MHz Bandwidth) 3 dB Roof Top

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 VHF 25-110 Watt Model Chart

M20KTS9PW1AN 136–174 MHz

Option	Description
G67AG	ADD: Screw, HP Remote Mount W4, W5, W7
G67AH	ADD: Screw, HP Remote Mount W3
G67AJ	ADD: Screw, HP Remote Mount W9
G67AM	ADD: Screw, HP Rem Mnt No CH W4, 5, 7, 9
G655AA	ADD: Quick Rel Remote Mount W3
G655AB	ADD: Quick Remote Mount W4, 5, 7
G655AC	ADD: Quick Rel Remote Mount W9
G655AD	ADD: Quick HP Rem Mnt No CH W4, 5, 7, 9
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hardware
G159AD	ADD: Encryption UCM HW 30 Sec Key Ret
W22AR	ADD: W9 Palm Microphone
W22AS	ADD: Hand Mic

Item No.	Description	G67AG	G67AH	G67AJ	G67AM	G655AA	G655AB	G655AC	G655AD	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W22AR	W22AS
HUD4025_	VHF 136-174 MHz 110W Main Board	X																
HKN6110_	Mobile Power Cable		X	X	X	X	X	X	X	X								
HHN4048_	Remote Housing Hardware Kit, Assy		X	X	X	X	X	X	X	X								
HLN4921_	Trunnion				X			X										
HLN4952_	Fuse Kit for GRN & ORG Leads		X		X			X										
HLN6231_	Hardware Remote Dash for 9000 Cable		X					X										
HLN6432_	Back Housing Kit		X					X										
HLN6862_	HHCH Remote Accessory Cable			X		X												
HLN6909_	Quick Release HP Trunnion					X	X	X	X									
HLN6910_	Thumb Screw HP XTL5000 Trunnion		X	X	X													
HMN4044_	Handheld Control Head									X								
AAHN4045_	W4 Control Head										X							
HLN6105_	Spare Button Kit										X	X	X					
HLN6688_	Spare Button Kit										X	X	X	X				
HLN6440_	W5 Control Head											X						
HLN6396_	CH DEK Compatible											X	X					
HLN6441_	W7 Control Head												X					
HCN1078_	W9 Control Head (Black)													X				
HLN6876_	Secure Interface Board 3-Day Key Retention														X			
NTN9738_	UCM Module														X	X		
HLN6877_	Secure Interface Board 30-Sec Key Retention															X		
HMN1061_	W9 Palm Microphone																X	
HMN1080_	Standard Palm Microphone W4, 5, 7																	X

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 VHF 25-110 Watt Model Chart (cont.)

M20KTS9PW1AN 136–174 MHz

Option	Description
W109CS	ALT: Microphone Handset with Hangup Cup
G110AB	INT: 17ft Control Head Cable W4, 5, 7, 9
G110AC	INT: W3 Remote Y Cable
B18CL	ADD: Auxiliary Speaker Spectra 5 Watt
W432AE	ENH: 10 Watt Audio (Standard on high power)
G296AA	ADD: Antenna 1/4 Wave Whip Roof Top 136-144 MHz
G297AA	ADD: Antenna 1/4 Wave Roof Top VHF 14 -150.8 MHz
G299AA	ADD: Antenna 1/4 Wave Roof Top 150.8 -162 MHz
G300AA	ADD: Antenna 1/4 Wave Roof Top 162 - 175 MHz
G301AA	ADD: 3 dB Antenna 136-174 MHz
W652AL	ADD: VHF Ant Broadband 136-162 MHz
G629AA	ADD: 1/4 Wave Broadband Ant 146-174
G792AA	ADD: VHF Ant Wideband 136-174 MHz

W109CS	G110AB	G110AC	B18CL	W432AE	G296AA	G297AA	G299AA	G300AA	G301AA	W652AL	G629AA	G792AA	Item No.	Description
X													HLN1220_	Microphone Handset with Hangup Clip
	X												HKN4356_	Standard 17’ CH Remote Cable
		X											HKN6096_	Handheld Control Head Y Cable
			X										HSN4031_	Speaker 5 Watt
				X									HSN4032_	Speaker 10 Watt
					X								HAD4006_	1/4 Wave Whip Roof Top 136-144 MHz
						X							HAD4007_	1/4 Wave Roof Top VHF 144-150.8 MHz
							X						HAD4008_	1/4 Wave Roof Top 150.8-162 MHz
								X					HAD4009_	1/4 Wave Roof Top 162-175 MHz
									X				RAD4010_	3dB Antenna 136-174 MHz
										X			HAD4016_	Broadband 136-162 MHz
											X		HAD4017_	1/4 Wave Broadband Antenna 146-174 MHz
												X	HAD4021_	Wideband 136-174 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 Motorcycle UHF Range 1 4-15 Watt Model Chart

M20QSS9PW1AN 380–470 MHz

Option	Description
G67AD	ADD: Remote Control Microphone W4, W5, W7
G67AF	ADD: Remote Mount No Control Head Needed
G82AA	ADD: Motorcycle W4 Control Head
G83AA	ADD: Motorcycle W5 Control Head
G84AA	ADD: Motorcycle W7 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W22AT	ADD: Hand Microphone (Motorcycle WP Mic)
W15AG	ADD: Black Weather Resistant Enclosure
G151AA	ADD: White Weather Resistant Enclosure
B18CM	ADD: Auxiliary Speaker Spec Motorcycle
G210AA	ADD: Motorcycle Antenna 1/4 Wave Whip 380-433 MHz
G283AA	ADD: Motorcycle Antenna 1/4 WAve Whip 450-482 MHZ

G67AD	G67AF	G82AA	G83AA	G84AA	G159AC	G159AD	W22AT	W15AG	G151AA	B18CM	G210AA	G283AA	Item No.	Description
X	X	X											HLN6863_	Accessory Connector
X													HUE4039A	UHF R1 380-470 MHz Main Board
	X	X											HLN6861_	Hardware Standard Install
	X												HLN6842_	Motorcycle Hardware 800 15 w w/W90
	X	X											HLN6884_	Motorcycle Interconnect Board
	X	X											HKN4191_	Mobile Power Cable
	X	X											HKN6062_	Motorcycle Control Head Cable 8’
			X										PMLN4019_	W4 Motorcycle Control Head
				X	X								HLN6105_	Spare Button Kit
				X	X								HLN6688_	Spare Button Kit
						X							HLN6876_	Secure Interface Board 3-Day Key Retention
							X						HLN6877_	Secure Interface Board 30-Sec Key Retention
								X					HMN1079_	Motorcycle Palm Microphone
										X			HSN6003_	Motorcycle Water Resistant Speaker
									X	X			HKN6032_	Motorcycle Power Cable
									X				HLN1445_	White Motorcycle Enclosure and Hardware
								X					HLN1446_	Black Motorcycle Enclosure and Hardware
											X		HAE6014_	Motorcycle Antenna 1/4 Wave Whip 380-433 MHz
												X	RAE4024ARB	Motorcycle Antenna 1/4 WAve Whip 450-482 MHZ

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 UHF Range 1 4-40 Watt Model Chart

M20QSS9PW1AN 380–470 MHz

Option	Description
G66AA	ADD: Dash Mount W4, W5, W7
G66AB	ADD: Dash Mount W3
G66AC	ADD: Dash Mount No Control Head Needed
G67AA	ADD: Remote Mount W4, W5, W7
G67AB	ADD: Remote Mount W9
G67AC	ADD: Remote Mount W3
G67AE	ADD: Remote Mount No Control Head
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W382AG	ALT: Control Station Palm Microphone
W665BE	ADD: Control Station Operation
G91AA	ADD: Control Station Power Supply

Item No.	Description	G66AA	G66AB	G66AC	G67AA	G67AB	G67AC	G67AE	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W382AG	W665BE	G91AA
HUE4039_	UHF R1 380-470 MHz Main Board	X																
HLN6861_	Installation Hardware		X	X	X	X	X	X	X									
HLN6863_	Accessory Connector Plug		X	X	X	X	X	X	X									
HKN4191_	Mobile Power Cable		X	X	X													
HLN6885_	Handheld CH Interconnect Board			X				X										
HLN6883_	Remote Interconnect Board					X	X		X									
HLN6813_	Control Head Trunnion Kit					X												
HLN6432_	Back Housing Kit					X												
HKN4192_	Mobile Power Cable 20 ft.					X	X	X	X									
HKN4356_	Standard 17 ft Control Head Remote Cable					X	X	X										
HKN6096_	Handheld Control Head Y Cable					X	X	X										
HLN4921_	Trunnion						X											
HMN4044_	Handheld Control Head								X									
HLN6105_	Spare Button Kit									X	X	X						
HLN6688_	Spare Button Kit									X	X	X						
HLN6396_	CH DEK Compatible										X	X						
HCN1078_	W9 Control Head												X					
HMN1050_	Control Station Microphone															X		
HLN6876_	Secure Interface Board 3-Day Key Retention													X				
HLN6877_	Secure Interface Board 30-Sec Key Retention														X			
HLN6042_	Base Tray																X	
HLN6047_	BDW Installation Base Tray																X	
HPN4001_	Control Station Power Supply																	X

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 UHF Range 1 4-40 Watt Model Chart (cont.)

M20QSS9PW1AN 380–470 MHz

Option	Description
W22AR	ADD: W9 Palm Microphone
W22AS	ADD: Hand Microphone
W109CS	ALT: Microphone Handset with Hangup Cup
B18CL	ADD: Auxiliary Spkr Spectra 5 Watt
W432AE	ENH: 10-Watt Audio (Standard on High Power)
G426AA	ADD: Antenna 1/4 Wave Whip 450-470 MHz
G428AA	ADD: Antenna 3.5 db 450-470 MHz
G430AA	ADD: Antenna 5.0 dB 450-470 MHz
G425AA	ADD: Antenna 1/4 Wave Whip 380-433 MHz
G427AA	ADD: Antenna 3.5 dB 380-433 MHz
G429AA	ADD: Antenna 5.0 dB 380-433 MHz
G431AA	ADD: Antenna Wideband 380-470 MHz

W22AR	W22AS	W109CS	B18CL	W432AE	G426AA	G428AA	G430AA	G425AA	G427AA	G429AA	G431AA	Item No.	Description
X												HMN1061_	W9 Palm Microphone
	X											HMN1080_	Standard Palm Microphone W4, W5, W7
		X										HLN1220_	Microphone Handset with Hangup Clip
			X									HSN4018_	Speaker 5 Watt
				X								HSN6001_	Speaker 10 Watt
					X							HAE4003_	Antenna, 1/4 Wave Whip, 450-470 MHz
						X						HAE4011_	Antenna, 3.5 dB, 450-470 MHz
							X					RAE4014_	Antenna, 5.0 dB, 450-470 MHz
								X				HAE6012_	Antenna, 1/4 Wave Whip, 380-433 MHz
									X			HAE6010_	Antenna, 3.5 dB, 380-433 MHz
										X		HAE6011_	Antenna, 5.0 dB, 380-433 MHz
											X	HAE6013_	Antenna, 2.0 dB Wideband, 380-470 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 UHF Range 1 25-110 Watt Model Chart

M20QTS9PW1AN 380–470 MHz

Option	Description
G67AG	ADD: Screw, HP Remote Mount W4, W5, W7
G67AH	ADD: Screw, HP Remote Mount W3
G67AJ	ADD: Screw, HP Remote Mount W9
G67AM	ADD: Screw, HP Rem Mnt No CH W4, 5, 7, 9
G655AA	ADD: Quick Rel Remote Mount W3
G655AB	ADD: Quick Remote Mount W4, W5, W7
G655AC	ADD: Quick Rel Remote Mount W9
G655AD	ADD: Quick, HP Rem Mnt No CH W4, 5, 7, 9
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hardware
G159AD	ADD: Encryption UCM HW 30 Sec Key Ret
W22AR	ADD: W9 Palm Microphone
W22AS	ADD: Hand Mic

Item No.	Description	G67AG	G67AH	G67AJ	G67AM	G655AA	G655AB	G655AC	G655AD	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W22AR	W22AS
HUE2202_	UHF R1 100W 380-470 MHz	X																
HKN6110_	Mobile Power Cable		X	X	X	X	X	X	X									
HHN4048_	Remote Housing Hardware Kit, Assy		X	X	X	X	X	X	X									
HLN4921_	Trunnion				X				X									
HLN4952_	Fuse Kit for GRN & ORG Leads		X		X			X										
HLN6231_	HDW Remote Dash for 9000 Cable		X					X										
HLN6432_	Back Housing Kit		X					X										
HLN6862_	HHCH Remote Accessory Cable			X		X												
HLN6909_	Quick Release HP Trunnion					X	X	X	X									
HLN6910_	Thumb Screw HP XTL5000 Trunnion		X	X	X	X												
HMN4044_	Handheld Control Head									X								
AAHN4045_	W4 Control Head										X							
HLN6105_	Spare Button Kit										X	X	X					
HLN6688_	Spare Button Kit										X	X	X	X				
HLN6440_	W5 Control Head											X						
HLN6396_	CH DEK Compatible											X	X					
HLN6441_	W7 Control Head												X					
HCN1078_	W9 Control Head (Black)													X				
HLN6876_	Secure Interface Board 3-Day Key Retention														X			
NTN9738_	UCM Module														X	X		
HLN6877_	Secure Interface Board 30-Sec Key Retention															X		
HMN1061_	W9 Palm Microphone																X	
HMN1080_	Standard Palm Microphone W4, 5, 7																	X

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 UHF Range 1 25-110 Watt Model Chart (cont.)

M20QTS9PW1AN 380–470 MHz

Option	Description
W109CS	ALT: Microphone Handset with Hangup Cup
G110AB	INT: 17 ft Control Head Cable W4, 5, 7, 9
G110AC	INT: W3 Remote Y Cable
B18CL	ADD: Auxiliary Spkr Spectra 5 Watt
W432AE	ENH: 10-Watt Audio (Standard on High Power)
G425AA	ADD: Antenna 1/4 Wave Whip 380-420 MHz
G426AA	ADD: Antenna 1/4 Wave 450-470 MHz
G427AA	ADD: Antenna 3.5 dB 380-420 MHz
G428AA	ADD: Antenna 3.5 dB 450-470 MHz
G429AA	ADD: Antenna 5.0 dB 380-420 MHz
G430AA	ADD: Antenna 5.0 dB 450-470 MHz
G431AA	ADD: Antenna Wideband 380-470 MHz

W109CS	G110AB	G110AC	B18CL	W432AE	G425AA	G426AA	G427AA	G428AA	G429AA	G430AA	G431AA	Item No.	Description
X												HLN1220_	Microphone Handset with Hangup Clip
	X											HKN4356_	Standard 17’ CH Remote Cable
		X										HKN6096_	Handheld Control Head Y Cable
			X									HSN4031_	Speaker 5 Watt
				X								HSN4032_	Speaker 10 Watt
					X							HAE6012_	1/4 Wave Whip 380-420 MHz P 136-144 MHz
						X						HAE4003_	1/4 Wave Whip 450-470 MHz
							X					RAE6010_	3.5 dB, 380-420 MHz
								X				HAE4011_	3.5 dB, 450-470 MHz
									X			HAE6011_	5.0 dB, 380-420 MHz
										X		RAE4014_	5.0 dB, 450-470 MHz
											X	HAE6013_	Wideband, 380-470 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 Motorcycle UHF Range 2 4-15 Watt Model Chart

M20SSS9PW1AN 450–520 MHz

Option	Description
G67AD	ADD: Remote Control Microphone W4, W5, W7
G67AF	ADD: Remote Mount No Control Head Needed
G82AA	ADD: Motorcycle W4 Control Head
G83AA	ADD: Motorcycle W5 Control Head
G84AA	ADD: Motorcycle W7 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W22AT	ADD: Hand Microphone (Motorcycle WP Mic)
W15AG	ADD: Black Weather Resistant Enclosure
G151AA	ADD: White Weather Resistant Enclosure
B18CM	ADD: Auxiliary Speaker Spec Motorcycle
G510AA	ADD: Antenna LowPro Motorcycle 450-512 MHz

G67AD	G67AF	G82AA	G83AA	G84AA	G159AC	G159AD	W22AT	W15AG	G151AA	B18CM	G510AA	Item No.	Description
X	X	X										HLN6863_	Accessory Connector
X												HUE4040A	UHF R2 450-520 MHz Main Board
	X	X										HLN6861_	Hardware Standard Install
	X											HLN6842_	Motorcycle Hardware 800 15 w w/W90
	X	X										HLN6884_	Motorcycle Interconnect Board
	X	X										HKN4191_	Mobile Power Cable
	X	X										HKN6062_	Motorcycle Control Head Cable 8'
			X									PMLN4019_	W4 Motorcycle Control Head
				X	X							HLN6105_	Spare Button Kit
				X	X							HLN6688_	Spare Button Kit
						X						HLN6876_	Secure Interface Board 3-Day Key Retention
							X					HLN6877_	Secure Interface Board 30-Sec Key Retention
								X				HMN1079_	Motorcycle Palm Microphone
										X		HSN6003_	Motorcycle Water Resistant Speaker
									X	X		HKN6032_	Motorcycle Power Cable
									X			HLN1445_	White Motorcycle Enclosure and Hardware
								X				HLN1446_	Black Motorcycle Enclosure and Hardware
											X	HAE6016_	Antenna, Low-Profile Motorcycle, 450-512 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 UHF Range 2 4-45 Watt Model Chart

M20SSS9PW1AN 450–520 MHz

Option	Description
G66AA	ADD: Dash Mount W4, W5, W7
G66AB	ADD: Dash Mount W3
G66AC	ADD: Dash Mount No Control Head Needed
G67AA	ADD: Remote Mount W4, W5, W7
G67AB	ADD: Remote Mount W9
G67AC	ADD: Remote Mount W3
G67AE	ADD: Remote Mount No Control Head
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W382AG	ALT: Control Station Palm Microphone
W665BE	ADD: Control Station Operation
G91AA	ADD: Control Station Power Supply

Item No.	Description	G66AA	G66AB	G66AC	G67AA	G67AB	G67AC	G67AE	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W382AG	W665BE	G91AA
HUE4040_	UHF R2 450-520 MHz Main Board	X																
HLN6861_	Installation Hardware		X	X	X	X	X	X	X									
HLN6863_	Accessory Connector Plug		X	X	X	X	X	X	X									
HKN4191_	Mobile Power Cable		X	X	X													
HLN6885_	Handheld CH Interconnect Board			X				X										
HLN6883_	Remote Interconnect Board					X	X		X									
HLN6813_	Control Head Trunnion Kit					X												
HLN6432_	Back Housing Kit					X												
HKN4192_	Mobile Power Cable 20 ft.					X	X	X	X									
HKN4356_	Standard 17 ft Control Head Remote Cable					X	X	X										
HKN6096_	Handheld Control Head Y Cable					X	X	X										
HLN4921_	Trunnion						X											
HMN4044_	Handheld Control Head								X									
HLN6105_	Spare Button Kit									X	X	X						
HLN6688_	Spare Button Kit									X	X	X						
HLN6396_	CH DEK Compatible										X	X						
HCN1078_	W9 Control Head												X					
HMN1050_	Control Station Microphone														X			
HLN6876_	Secure Interface Board 3-Day Key Retention													X				
HLN6877_	Secure Interface Board 30-Sec Key Retention														X			
HLN6042_	Base Tray																X	
HLN6047_	BDW Installation Base Tray																X	
HPN4001_	Control Station Power Supply																	X

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 UHF Range 2 4-45 Watt Model Chart (cont.)

M20SSS9PW1AN 450–520 MHz

Option	Description
W22AR	ADD: W9 Palm Microphone
W22AS	ADD: Hand Microphone
W109CS	ALT: Microphone Handset with Hangup Cup
B18CL	ADD: Auxiliary Spkr Spectra 5 Watt
W432AE	ENH: 10-Watt Audio (Standard on High Power)
G426AA	ADD: Antenna 1/4 Wave Whip 450-470 MHz
G428AA	ADD: Antenna 3.5 db 450-470 MHz
G430AA	ADD: Antenna 5.0 dB 450-470 MHz
G486AA	ADD: Antenna 5.0 dB Gain 494-512 MHz
G490AB	ADD: Antenna 1/4 Wave Whip 470-512 MHz
G493AB	ADD: Antenna 3 dB Roof Top 470-495 MHz
G494AB	ADD: Antenna 3 dB Roof Top 494-512 MHz
G511AA	ADD: Antenna 2 dB Wide Band 450-520 MHz
W124AR	ADD: Antenna 5.0 dB Gain 470-494 MHz
G510AA	ADD: Antenna Low Propfile 450-512 Mhz

W22AR	W22AS	W109CS	B18CL	W432AE	G426AA	G428AA	G430AA	G486AA	G490AB	G493AB	G494AB	G511AA	W124AR	G510AA	Item No.	Description
X															HMN1061_	W9 Palm Microphone
	X														HMN1080_	Standard Palm Microphone W4, W5, W7
		X													HLN1220_	Microphone Handset with Hangup Clip
			X												HSN4018_	Speaker 5 Watt
				X											HSN6001_	Speaker 10 Watt
					X										HAE4003_	Antenna, 1/4 Wave Whip, 450-470 MHz
						X									HAE4011_	Antenna, 3.5 dB, 450-470 MHz
							X								RAE4014_	Antenna, 5.0 dB, 450-470 MHz
													X		RAE4015_	Antenna, 5.0 dB, 470-494 MHz
								X							RAE4016_	Antenna 5.0 dB Gain 494-512 MHz
									X						HAE4004_	Antenna 1/4 Wave Whip 470-512 MHz
										X					HAE4012_	Antenna 3 dB Roof Top 470-495 MHz
											X				HAE4013_	Antenna 3 dB Roof Top 494-512 MHz
												X			HAE6015_	Antenna 2 dB Wide Band 450-520 MHz
														X	HAE6016_	Antenna Low Propfile 450-512 Mhz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 Motorcycle 700-800 MHz 3.5-15 Watt Model Chart

M20URS9PW1AN 764–870 MHz

Option	Description
G67AD	ADD: Remote Control Microphone W4, W5, W7
G67AF	ADD: Remote Mount No Control Head Needed
G82AA	ADD: Motorcycle W4 Control Head
G83AA	ADD: Motorcycle W5 Control Head
G84AA	ADD: Motorcycle W7 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W22AT	ADD: Hand Microphone (Motorcycle WP Mic)
W15AG	ADD: Black Weather Resistant Enclosure
G151AA	ADD: White Weather Resistant Enclosure
B18CM	ADD: Auxiliary Speaker Spec Motorcycle
G335AU	ADD: Antenna 3 dB Motorcycle 764-870 MHz
G174AB	ADD: Antenna 3 dB LowPro Motorcycle 764-870 MHz

G67AD	G67AF	G82AA	G83AA	G84AA	G159AC	G159AD	W22AT	W15AG	G151AA	B18CM	G335AU	G174AB	Item No.	Description
X	X	X											HLN6863_	Accessory Connector
X													HUF4017_	700-800 MHz Main Board
	X	X											HLN6861_	Hardware Standard Install
	X												HLN6842_	Motorcycle Hardware 800 15 w w/W90
	X	X											HLN6884_	Motorcycle Interconnect Board
	X	X											HKN4191_	Mobile Power Cable
	X	X											HKN6062_	Motorcycle Control Head Cable 8’
			X										PMLN4019_	W4 Motorcycle Control Head
				X	X								HLN6105_	Spare Button Kit
				X	X								HLN6688_	Spare Button Kit
						X							HLN6876_	Secure Interface Board 3-Day Key Retention
							X						HLN6877_	Secure Interface Board 30-Sec Key Retention
								X					HMN1079_	Motorcycle Palm Microphone
										X			HSN6003_	Motorcycle Water Resistant Speaker
									X	X			HKN6032_	Motorcycle Power Cable
										X			HLN1445_	White Motorcycle Enclosure and Hardware
								X					HLN1446_	Black Motorcycle Enclosure and Hardware
											X		HAF4015_	Antenna, 3 dB Motorcycle, 764-870 MHz
												X	HAF4018_	Antenna, 3 dB Low-Profile Motorcycle, 764-870 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

ASTRO XTL 5000 700-800 MHz 3.5-35 Watt Model Chart

M20URS9PW1AN 764–870 MHz

Option	Description
G66AA	ADD: Dash Mount W4, W5, W7
G66AB	ADD: Dash Mount W3
G66AC	ADD: Dash Mount No Control Head Needed
G67AA	ADD: Remote Mount W4, W5, W7
G67AB	ADD: Remote Mount W9
G67AC	ADD: Remote Mount W3
G67AE	ADD: Remote Mount No Control Head
G72AA	ADD: W3 Handheld Control Head
G73AA	ADD: W4 Control Head
G79AA	ADD: W5 Control Head
G80AA	ADD: W7 Control Head
G81AA	ADD: W9 Control Head
G159AC	ADD: Encryption UCM Hdw 3-Day Key Ret
G159AD	ADD: Encryption UCM Hdw 30-Sec Key Ret
W382AG	ALT: Control Station Palm Microphone
W665BE	ADD: Control Station Operation
G91AA	ADD: Control Station Power Supply

G66AA	G66AB	G66AC	G67AA	G67AB	G67AC	G67AE	G72AA	G73AA	G79AA	G80AA	G81AA	G159AC	G159AD	W382AG	W665BE	G91AA	Item No.	Description
X																	HUF4017_	700-800 MHz Main Board
	X	X	X	X	X	X	X										HLN6861_	Hardware Standard Install
	X	X	X	X	X	X	X										HLN6863_	Accessory Connector
	X	X	X														HKN4191_	Mobile Power Cable
		X				X											HLN6885_	Handheld CH Interconnect Board
				X	X		X										HLN6883_	Remote Interconnect Board
				X													HLN6813_	Control Head Trunnion Kit
				X													HLN6432_	Back Housing Kit
				X	X	X	X										HKN4192_	Mobile Power Cable 20 ft.
				X	X	X											HKN4356_	Standard 17 ft Control Head Remote Cable
					X												HLN4921_	Trunnion
							X										HMN4044_	Handheld Control Head
								X	X	X							HLN6105_	Spare Button Kit
								X	X	X							HLN6688_	Spare Button Kit
									X	X							HLN6396_	CH DEK Compatible
											X						HCN1078_	W9 Control Head
												X					HLN6876_	Secure Interface Board 3-Day Key Retention
													X				HLN6877_	Secure Interface Board 30-Sec Key Retention
														X			HMN1050_	Control Station Microphone
															X		HLN6042_	Mobile DeskTray
															X		HLN6047_	Hardware Installation Base Tray
																X	HPN4001_	Control Station Power Supply

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

(Chart continued on the next page)

ASTRO XTL 5000 700-800 MHz 3.5-35 Watt Model Chart (cont.)

M20URS9PW1AN 764–870 MHz

Option										Description
W22AR										ADD: W9 Palm Microphone
	W22AS									ADD: Hand Microphone
		W109CS								ALT: Microphone Handset with Hangup Cup
			B18CL							ADD: Auxiliary Spkr Spectra 5 Watt
				W432AE						ENH: 10-Watt Audio (Standard on High Power)
					W484AD					ADD: Antenna 3 dB Gain (764-870 MHz)
						G335AT				ADD: Antenna 1/4 Wave 764-870 MHz
							G174AA			ADD: Antenna 3 dB Low-Profile 764-870 MHz
								G175AA		ADD: Antenna 3 dB Elevat Feed 764-870 MHz
									Item No.	Description
	X								HMN1061_	W9 Palm Microphone
		X							HMN1080_	Standard Palm Microphone W4,5,7
			X						HLN1220_	Microphone Handset with Hangup Clip
				X					HSN4018_	Speaker 5 Watt
					X				HSN6001_	Speaker 10 Watt
						X			HAF4017_	Antenna, 3 dB Gain, 764-870 MHz
							X		HAF4016_	Antenna, 1/4 Wave, 764-870 MHz
								X	HAF4013_	Antenna, 3 dB Low Profile, 764-870 MHz
									HAF4014_	Antenna, 3 dB Elevated Feed, 764-870 MHz

X = Item Included
_ = the latest version kit. When ordering a kit, refer to your specific kit for the suffix number.

VHF Radio Specifications

GENERAL

FCC Designations: AZ492FT3806
AZ492FT3808

Temperature Range:
Operating: –30°C to +60°C
Storage: –55°C to +85°C

Power Supply: 12 Vdc Negative Ground Only

Battery Drain: (Maximum)
50 Watt:
Standby @ 13.8 V: 0.8 A
Receive at Rated Audio @ 13.6 V: 3.0 A
Transmit @ Rated Power:
10 W 8.0 A
50 W 13.0 A

100 Watt:
Standby @ 13.4 V: 0.8 A
Receive at Rated Audio @ 13.4 V: 3.2 A
Transmit @ Rated Power:
100 W 20.0 A

Mid Power Dimensions (H x W x D)
W4, W5, and W7 Models:
Remote-Mount Control Head: 2.0" x 7.1"x 2.2"
(50.8 mm x 180.3 mm x 55.9 mm)
Dash-Mount Radio: 2.0" x 7.1"x 9.1"
(50.8 mm x 180.3 mm x 218.4 mm)

W9 Model:
Remote-Mount Control Head: 3.4" x 6.5"x 1.7"
(86.4 mm x 165.1 mm x 43.2 mm)
Speaker: (excluding mounting bracket)
5.5" x 5.5"x 2.5"
(139.7 mm x 139.7 mm x 63.5 mm)

Mid Power Weight:
Radio: 5.1 lbs (2.3 kg)
Speaker: 1.5 lbs (0.7 kg)

High Pwr Dimensions wtih Handle(H x W x D)
2.65” x 8.08” x 12.31”
(67.31 mm x 205.13 mm x 312.6 mm)

High Power Weight with Handle
8.8 lbs (4 kg)

RECEIVER

Frequency Range:
Range 1: 136–174 MHz

Channel Spacing: 12.5 kHz/25 kHz

Input Impedance: 50 Ohm

Frequency Separation: Full Bandsplit

Sensitivity: (per EIA spec. RS204C)
With pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing): 0.25 µV
12 dB SINAD: (25 kHz Channel Spacing): 0.20 µV
Without pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing): 0.4 µV
12 dB SINAD: (25 kHz Channel Spacing): 0.3 µV

Intermodulation: (per EIA Specifications)
With pre-amplifier
(Measured in the Analog Mode): –80 dB
Without pre-amplifier
(Measured in the Analog Mode): –85 dB

Digital Sensitivity:
With pre-amplifier
1% BER (12.5 kHz channel): 0.25 µV
5% BER (12.5 kHz channel): 0.20 µV
Without pre-amplifier
1% BER (12.5 kHz channel): 0.4 µV
5% BER (12.5 kHz channel): 0.3 µV

Selectivity: (per EIA Specifications)
(Measured in the Analog Mode)
25 kHz Channel Spacing: –90 dB
12.5 kHz Channel Spacing: –70 dB

Intermodulation: (per EIA Specifications)
(Measured in the Analog Mode): –80 dB

Spurious Rejection: –90 dB

Frequency Stability:
(–30° to +60°C; 25°C Reference): ±348 Hz @ 174 MHz

Audio Output: (per EIA Specifications)
(Measured in the Analog Mode):
5 Watts at Less Than 3% Distortion
10 Watts Optional with Reduced Duty Cycle
13 Watts for High-Power Radios

TRANSMITTER

Frequency Range:
Range 1: 136–174 MHz

Rated Output Power:
Low-Power Radio: 25 Watt
Mid-Power Radio: 50 Watt
High-Power Radio: 100 Watt

Channel Spacing: 12.5 kHz or 25 kHz

Output Impedance: 50 Ohm

Frequency Separation:
Range 1: 30 MHz

Frequency Stability:
(–30° to +60°C; 25°C Ref.): ±348 Hz @ 174 MHz

Modulation Limiting:
25 kHz Channel Spacing: ±5.0 kHz
12.5 kHz Channel Spacing: ±2.5 kHz

Modulation Fidelity (C4FM):
12.5 kHz Digital Channel: ±2.8 kHz

FM Hum and Noise:
25 kHz Channel Spacing: –50 dB
12.5 kHz Channel Spacing: –40 dB

Emission (Conduct/Radiated): –85 dBc/-20dBm

Audio Sensitivity:
(For 60% Max. Deviation at 1 kHz): 0.08V ±3 dB

Audio Response:
(Measured in the Analog Mode)
(6 dB/Octave Pre-Emphasis 300 to 3000Hz): +1, –3 dB

Audio Distortion:
(For 60% Max. Deviation at 1 kHz): 3% TIA 603

Emissions Designators:
8K10F1E, 11K0F3E, 15K0F2D, 16K0F3E, 20K0F1E, 15K0F1D, 11K0F1D, and 11K0F2D

Specifications subject to change without notice.
All measurements are taken in the test mode at 25 kHz channel spacing except where indicated.

UHF Range 1 Radio Specifications

GENERAL

FCC Designations: **AZ492FT4862**
AZ492FT4870

Temperature Range:
Operating: –30°C to +60°C
Storage: –51°C to +85°C

Power Supply: 12 Vdc Negative Ground Only

Battery Drain: (Maximum)
Standby @ 13.8 V: 0.85 A
Receive at Rated Audio @ 13.8 V: 3.2 A
Transmit @ Rated Power:
10 W 8.0 A
40 W 11.0 A

100 Watt:
Standby @ 13.4 V: 0.85 A
Receive at Rated Audio @ 13.4 V: 3.2 A
Transmit @ Rated Power:
100 W 24.0 A

Mid Power Dimensions (H x W x D)
W4, W5, and W7 Models:
Remote-Mount Control Head: 2.0" x 7.1"x 2.2"
(50.8 mm x 180.3 mm x 55.9 mm)
Dash-Mount Radio: 2.0" x 7.1"x 9.1"
(50.8 mm x 180.3 mm x 218.4 mm)

W9 Model:
Remote-Mount Control Head: 3.4" x 6.5"x 1.7"
(86.4 mm x 165.1 mm x 43.2 mm)
Speaker: (excluding mounting bracket)
5.5" x 5.5"x 2.5"
(139.7 mm x 139.7 mm x 63.5 mm)

Mid Power Weight:
Radio: 5.1 lbs (2.3 kg)
Speaker: 1.5 lbs (0.7 kg)

High Pwr Dimensions with Handle (H x W x D)
2.65" x 8.08" x 12.31"
(67.31 mm x 205.13 mm x 312.6 mm)

High Power Weight with Handle
8.8 lbs (4 kg)

RECEIVER

Frequency Range:
Range 1: 380–470 MHz

Channel Spacing: 12.5 kHz/20 kHz/25 kHz

Input Impedance: 50 Ohm

Frequency Separation: Full Bandsplit

Sensitivity: (per EIA spec. RS204C)
With pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing):
0.25 µV
12 dB SINAD: (25 kHz Channel Spacing):
0.20 µV
Without pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing):
0.4 µV
12 dB SINAD: (25 kHz Channel Spacing):
0.3 µV

Intermodulation: (per EIA Specifications)
With pre-amplifier
(Measured in the Analog Mode): –80 dB
Without pre-amplifier
(Measured in the Analog Mode): –85 dB

Digital Sensitivity:
With pre-amplifier
1% BER (12.5 kHz channel): 0.25 µV
5% BER (12.5 kHz channel): 0.20 µV
Without pre-amplifier
1% BER (12.5 kHz channel): 0.4 µV
5% BER (12.5 kHz channel): 0.3 µV

Selectivity: (per EIA Specifications)
(Measured in the Analog Mode)
25 kHz Channel Spacing: –82 dB
12.5 kHz Channel Spacing: –75 dB

Spurious Rejection: –90 dB

Frequency Stability:
(–30° to +60°C; 25°C Reference): ±0.0002%

Audio Output: (per EIA Specifications)
(Measured in the Analog Mode):
7.5 Watts at Less Than 3% Distortion
13 Watts Optional with Reduced Duty Cycle
13 Watts for High-Power Radios

TRANSMITTER

Frequency Range:
Range 1: 380–470 MHz

Rated Output Power:
Low-Power Radio: 25 Watt
Mid-Power Radio: 50 Watt
High-Power Radio: 100 Watt

Channel Spacing: 12.5 kHz or 25 kHz

Output Impedance: 50 Ohm

Frequency Separation: Full Bandsplit

Frequency Stability:
(–30° to +60°C; 25°C Ref.): ±0.0002%

Modulation Limiting:
25 kHz Channel Spacing: ±5.0 kHz
12.5 kHz Channel Spacing: ±4.0 kHz
12.5 kHz Channel Spacing: ±2.5 kHz

Modulation Fidelity (C4FM):
12.5 kHz Digital Channel: ±2.8 kHz

FM Hum and Noise:
25 kHz Channel Spacing: –45 dB
12.5 kHz Channel Spacing: –40 dB

Emission (Conduct/Radiated): –85 dBc/-20dBm

Audio Sensitivity:
(For 60% Max. Deviation at 1 kHz): 0.08V ±3 dB

Audio Response:
(Measured in the Analog Mode)
(6 dB/Octave Pre-Emphasis 300 to 3000Hz):
+1, –3 dB

Audio Distortion:
(For 60% Max. Deviation at 1 kHz): 3% TIA 603

Emissions Designators:
8K10F1E, 11K0F3E, 15K0F2D, 16K0F3E, 20K0F1E, 15K0F1D, 11K0F1D, and 11K0F2D

Specifications subject to change without notice.
All measurements are taken in the test mode at 25 kHz channel spacing except where indicated.

UHF Range 2 Radio Specifications

GENERAL

FCC Designations: AZ492FT4867

Temperature Range:
Operating: –30°C to +60°C
Storage: –51°C to +85°C

Power Supply: 12 Vdc Negative Ground Only

Battery Drain: (Maximum)
Standby @ 13.8 V: 0.85 A
Receive at Rated Audio @ 13.8 V: 3.2 A
Transmit @ Rated Power:
10 W 8.0 A
45 W 11.0 A

Dimensions (H x W x D)
W4, W5, and W7 Models:
Remote-Mount Control Head: 2.0" x 7.1"x 2.2"
(50.8 mm x 180.3 mm x 55.9 mm)
Dash-Mount Radio: 2.0" x 7.1"x 9.1"
(50.8 mm x 180.3 mm x 218.4 mm)

W9 Model:
Remote-Mount Control Head: 3.4" x 6.5"x 1.7"
(86.4 mm x 165.1 mm x 43.2 mm)
Speaker: (excluding mounting bracket)
5.5" x 5.5"x 2.5"
(139.7 mm x 139.7 mm x 63.5 mm)

Weight:
Radio: 5.1 lbs (2.3 kg)
Speaker: 1.5 lbs (0.7 kg)

RECEIVER

Frequency Range:
Range 2: 450–520 MHz

Channel Spacing: 12.5 kHz/20 kHz/25 kHz

Input Impedance: 50 Ohm

Frequency Separation: Full Bandsplit

Sensitivity: (per EIA spec. RS204C)
With pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing): 0.25 µV
12 dB SINAD: (25 kHz Channel Spacing): 0.20 µV
Without pre-amplifier
20 dB Quieting: (25 kHz Channel Spacing): 0.4 µV
12 dB SINAD: (25 kHz Channel Spacing): 0.3 µV

Intermodulation: (per EIA Specifications)
With pre-amplifier
(Measured in the Analog Mode): –80 dB
Without pre-amplifier
(Measured in the Analog Mode): –85 dB

Digital Sensitivity:
With pre-amplifier
1% BER (12.5 kHz channel): 0.25 µV
5% BER (12.5 kHz channel): 0.20 µV
Without pre-amplifier
1% BER (12.5 kHz channel): 0.4 µV
5% BER (12.5 kHz channel): 0.3 µV

Selectivity: (per EIA Specifications)
(Measured in the Analog Mode)
25 kHz Channel Spacing: –82 dB
12.5 kHz Channel Spacing: –75 dB

Spurious Rejection: –90 dB

Frequency Stability:
(–30° to +60°C; 25°C Reference): ±0.0002%

Audio Output: (per EIA Specifications)
(Measured in the Analog Mode):
7.5 Watts at Less Than 3% Distortion
13 Watts Optional with Reduced Duty Cycle
13 Watts for High-Power Radios

TRANSMITTER

Frequency Range:
Range 2: 450–520 MHz

Rated Output Power:
Mid-Power Radio:
45 Watt 450–500 MHz
40 Watt 500–512 MHz
25 Watt 512–520 MHz

Channel Spacing: 12.5 kHz or 25 kHz

Output Impedance: 50 Ohm

Frequency Separation: Full Bandsplit

Frequency Stability:
(–30° to +60°C; 25°C Ref.): ±0.0002%

Modulation Limiting:
25 kHz Channel Spacing: ±5.0 kHz
12.5 kHz Channel Spacing: ±4.0 kHz
12.5 kHz Channel Spacing: ±2.5 kHz

Modulation Fidelity (C4FM):
12.5 kHz Digital Channel: ±2.8 kHz

FM Hum and Noise:
25 kHz Channel Spacing: –45 dB
12.5 kHz Channel Spacing: –40 dB

Emission (Conducted and Radiated): –85 dBc

Audio Sensitivity:
(For 60% Max. Deviation at 1 kHz): 0.08V ±3 dB

Audio Response:
(Measured in the Analog Mode)
(6 dB/Octave Pre-Emphasis 300 to 3000Hz):
+1, –3 dB

Audio Distortion:
(For 60% Max. Deviation at 1 kHz): 2% TIA 603

Emissions Designators:
8K10F1E, 11K0F3E, 15K0F2D, 16K0F3E, 20K0F1E, 15K0F1D, 11K0F1D, and 11K0F2D

Specifications subject to change without notice.
All measurements are taken in the test mode at 25 kHz channel spacing except where indicated.

700–800 MHz Radio Specifications (Mid Power Models Only)

GENERAL

FCC Designations: AZ492FT5823

Temperature Range:
- Operating: –30° C to +60° C
- Storage: –40° C to +85° C

Power Supply: 12 Vdc Negative Ground Only

Battery Drain: (Maximum)
35 W:
- Standby @ 13.8 V: 0.7 A
- Receive at Rated Audio @ 13.8 V: 3.0 A
- Transmit @ Rated Power:
  - 35 W 12.0 A

Dimensions (H x W x D)
W4, W5, and W7 Models:
- Remote-Mount Control Head: 2.0" x 7.1"x 2.2" (50.8 mm x 180.3 mm x 55.9 mm)
- Dash-Mount Radio: 2.0" x 7.1"x 9.1" (50.8 mm x 180.3 mm x 231.1 mm)

W9 Model:
- Remote-Mount Control Head: 3.4" x 6.5"x 1.7" (86.4 mm x 165.0 mm x 43.2 mm)

Speaker: (excluding mounting bracket) 5.5" x 5.5"x 2.5" (139.7 mm x 139.7 mm x 63.5 mm)

Weight:
- Radio: 6.1 lbs (2.8 kg)
- Speaker: 1.5 lbs (0.7 kg)

RECEIVER

Frequency Range:
- 700 MHz Band: 764–776 MHz
- 800 MHz Band: 851–870 MHz

Channel Spacing: 12.5 kHz/20 kHz/25 kHz

Input Impedance: 50 ohm

Frequency Separation: Full Bandsplit

Sensitivity:
20 dB Quieting:
- 25 kHz Channel Spacing: 0.30 µV

12 dB SINAD:
- 25 kHz Channel Spacing: 0.25 µV

Digital Sensitivity:**
- 1% BER (12.5 kHz channel): 0.30 µV
- 5% BER (12.5 kHz channel): 0.25 µV

Adjacent Channel Selectivity*:
- 25 kHz Channel: 80 dB
- 12.5 kHz Channel: 65 dB

Intermodulation*: 80 dB

Spurious Rejection*: 90 dB

Frequency Stability*:
- (–30° to +60° C; 25° C Ref.): ±0.00015%

Audio Output at 3% Distortion*:
- 7.5 Watts into 8 Ohms
- 13 Watts into 3.2 Ohms

TRANSMITTER

Frequency Range:
700 MHz Band:
- Repeater Mode: 794–806 MHz
- Talkaround Mode: 764–776 MHz

800 MHz Band:
- Repeater Mode: 806–825 MHz
- Talkaround Mode: 851–870 MHz

Rated Output Power:
- 764–806 MHz Band: 2***/30 W
- 806–870 MHz Band: 35 W

Channel Spacing: 12.5 kHz/20 kHz/25 kHz

Output Impedance: 50 ohm

Frequency Separation: Full Bandsplit

Frequency Stability*:
- (–30° to +60°C; 25°C Ref.): ±0.00015%

Modulation Limiting*:
- 25 kHz Channel Spacing: ±5.0 kHz
- 12.5 kHz Channel Spacing: ±2.5 kHz

Modulation Fidelity (C4FM):**
- 12.5 kHz Digital Channel: ±2.8 kHz

FM Hum and Noise*:
- 20/25 kHz Channel: –40 dB
- 12.5 kHz Channel: –34 dB

Emission (Conducted and Radiated): –70 dBc/–85 dBc (GNSS)

Audio Sensitivity*:
(For 60% Max. Deviation at 1 kHz): 0.08 V ±3 dB

Audio Response*:
(6 dB/Octave Pre-Emphasis 300 to 3000 Hz): +1,–3 dB

Audio Distortion*: 2%

Emissions Designators:
8K10F1D, 8K10F1E, 11K0F3E, 16K0F3E, and 20K0F1E

Specifications subject to change without notice.
** Measured in analog mode per TIA/EIA 603 under nominal conditions.*
*** Measured in digital mode per TIA/EIA IS 102.CAAB.*
**** 2 W. itinerant frequencies.*

Notes

Chapter 1 Introduction

1.1 Notations Used in This Manual

Throughout the text in this publication, you will notice the use of warnings, cautions, and notes. These notations are used to emphasize that safety hazards exist, and care must be taken and observed.

NOTE: The Note notation indicates an operational procedure, practice, or condition that is essential to emphasize.

CAUTION indicates a potentially hazardous situation which, if not avoided, might result in equipment damage.

WARNING indicates a potentially hazardous situation which, if not avoided, could result in death or injury.

DANGER indicates an imminently hazardous situation which, if not avoided, will result in death or injury.

1.2 General

This manual includes all the information necessary to maintain peak product performance and maximum working time. This detailed level of service (component-level) is typical of some service centers, self-maintained customers, and distributors.

Use this manual in conjunction with the *ASTRO Digital XTL 5000 VHF/UHF Range 1/UHF Range 2/ 700–800 MHz Mobile Radio Basic Service Manual* (Motorola part number 6881096C73), which helps in troubleshooting a problem to a particular board.

Conduct the basic performance checks first to verify the need to analyze the radio and help pinpoint the functional problem area. In addition, you will become familiar with the radio test mode of operation which is a helpful tool. If any basic receiver or transmitter parameters fail to be met, the radio should be aligned using the radio alignment procedure described in the *ASTRO Digital XTL 5000 VHF/UHF Range 1/UHF Range 2/700–800 MHz Mobile Radio Basic Service Manual*.

Included in other areas of this manual are functional block diagrams, detailed theory of operation, troubleshooting charts and waveforms, schematics, and parts list. You should be familiar with these sections to aid in deducing the problem circuit. Also included are component location diagrams to aid in locating individual circuit components, as well as IC diagrams, which identify some convenient probe points.

The Theory of Operation section of this manual contains detailed descriptions of operations of many circuits. Once you locate the problem area, review the Troubleshooting Chart for that circuit to fix the problem.

Chapter 2 Product Overview

2.1 Introduction

The ASTRO Digital XTL 5000 radio is a dual-mode (trunked/conventional), microcontroller-based transceiver incorporating a Digital Signal Processor (DSP). The microcontroller handles the general radio control, monitors status, and processes commands input from the keypad or other user controls. The DSP processes the typical analog signals and generates the standard signaling digitally to provide compatibility with existing analog systems. In addition it provides for digital modulation techniques utilizing voice encoding techniques with error correction schemes to provide the user with enhanced range and audio quality all in a reduced bandwidth channel requirement. It allows embedded signaling which can mix system information and data with digital voice to add the capability of supporting a multitude of system features.

The XTL 5000 radios are wideband, synthesized, fixed-tuned radios and are available in the VHF (136–174 MHz), UHF Range 1 (380–470 MHz), UHF Range 2 (450–520 MHz), 700 MHz, and 800 MHz bands. All XTL 5000 radios are capable of both analog operation (12.5 kHz, 20 kHz, and 25 kHz bandwidths) and ASTRO mode operation (12.5 kHz bandwidth).

NOTE: The UHF radio does not support 20 kHz bandwidth.

2.2 Functional Blocks

The XTL 5000 radios contain the following functional blocks:

- Control-Head Assembly (Dash- or Remote-Mount)—is connected directly to the front of the transceiver or remotely by the interconnect board and control cable. This assembly contains a vacuum fluorescent (VF) display, VF driver, microprocessor and serial bus interface.
- Radio Power Distribution—contains voltage-regulation circuitry for power distribution throughout the radio.
- Receiver Front-End section—contains the preselector, low-noise amplifier (LNA), and mixer.
- Receiver Back-End section—contains the receiver intermediate-frequency (IF) amplifier/filter and the digital receiver back-end integrated circuit (IC).
- Transmitter section—contains the antenna switch, directional coupler/ detector, and power amplifier circuitry.
- Frequency Generation section—contains the synthesizer, voltage controlled oscillators (VCOs), reference oscillator, and receive and transmit buffers.
- Controller section—combines a vocoder and a controller into a single section containing the following elements:

2.3 Control-Head Assembly

This section discusses the basic operation and components of each control-head assembly.

2.3.1 Display, Vacuum Fluorescent Display Driver, Vacuum Fluorescent Voltage Source, Controls and Indicators, Status LEDs and Backlight LEDs

For information on the above, please refer to:

- W3 Control Head User's Guide, 6881096C67 and
- W4, W5, W7 and W9 Control Heads User's Guide, 6881096C68.

2.3.2 Vehicle Interface Ports

The Vehicle Interface Ports (VIPs) allow the control head to activate external circuits and receive inputs from the outside world. In general, VIP outputs are used for relay control, and VIP inputs accept inputs from external switches. The VIP IN and VIP OUT lines move as the configuration changes from Dash, to Remote, to Remote plus DEK. See the cable kit section for typical connections of VIP input switches and VIP output relays.

2.3.2.1 Dash-Mount Control-Head Configuration (Mid Power Only)

In the dash-mount configuration (Figure 2-1), only two VIP output pins are available, and they are located at the 26-pin accessory connector, J2-18 and J2-19. VIP input lines are not available in this configuration.

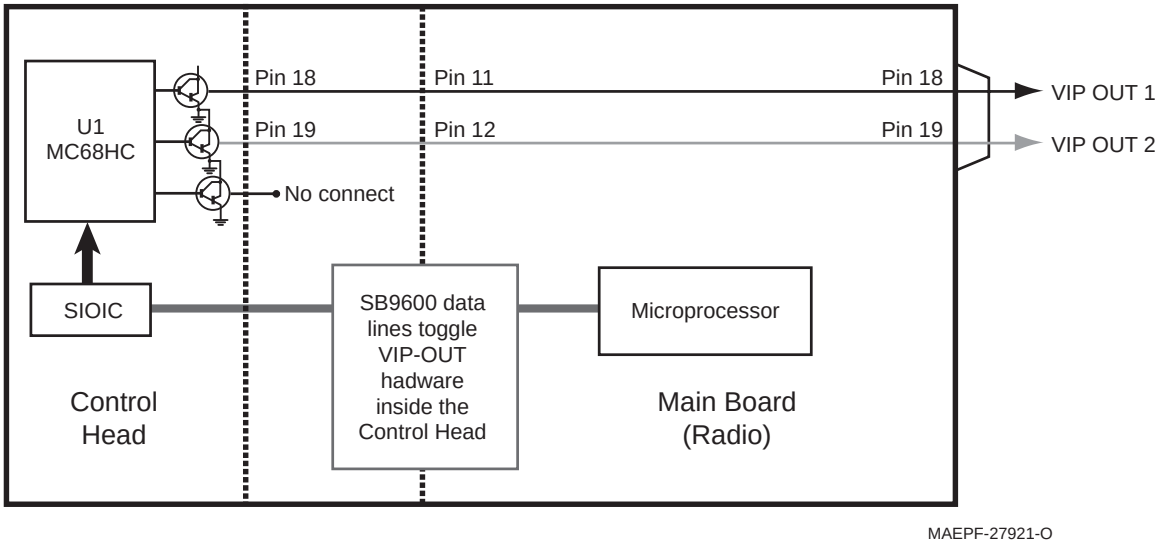

Figure 2-1. VIP Dash-Mount Configuration

2.3.2.2 Remote-Mount Standard Control-Head Configuration

Once the radio is put into a remote-mount configuration (Figure 2-2 on page 2-3), the two VIP output pins located at the rear connector (J2) stop functioning, and the VIP output pins located on the back of the control head below the area labeled "VIP" become the new VIP output pins. These connections are used to control relays, just as in the dash-mount configuration. One end of the relay should be connected to SWB+, while the other side is connected to VIP IN or VIP OUT pins (these pins are software-controlled on/off switches via transistors inside the control head or on the interconnect board).

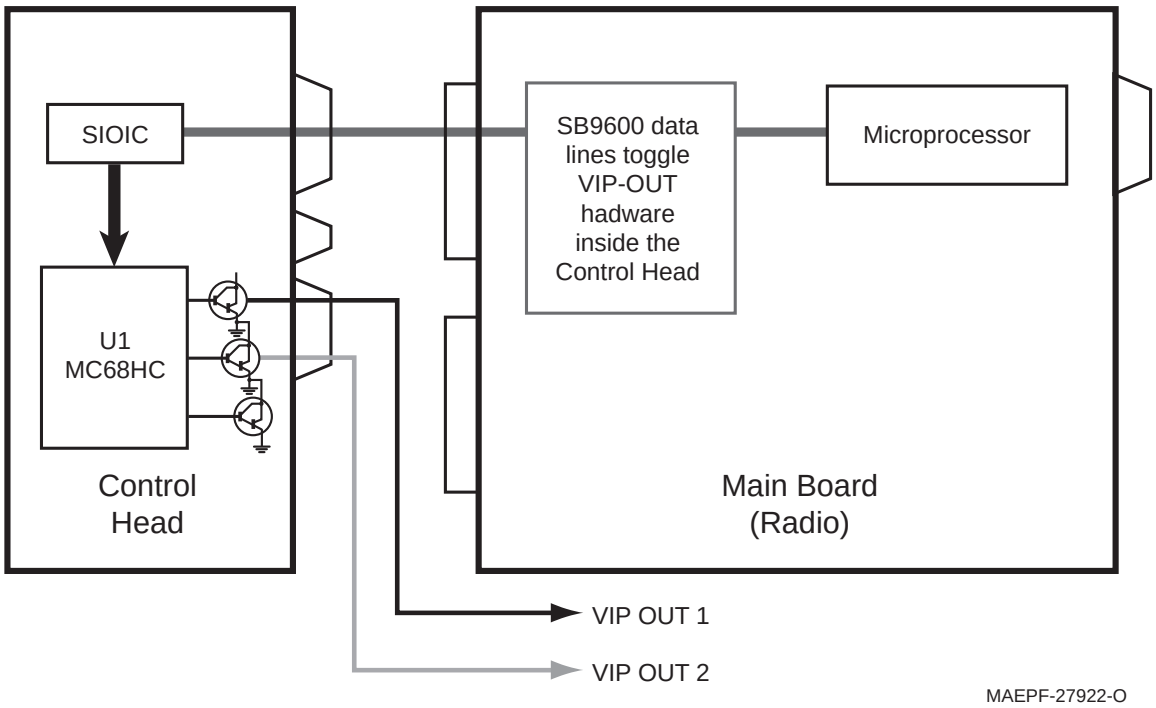

Figure 2-2. VIP Remote-Mount Configuration

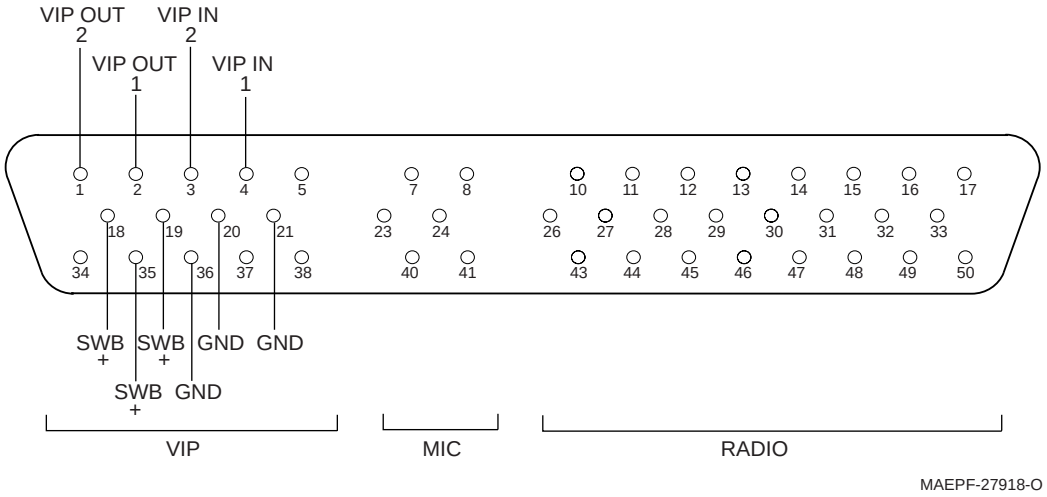

Figure 2-3. VIP Remote-Mount Pin-Outs (Male)

2.3.2.3 Remote-Mount W3 Hand-Held Control Head Configuration

Because the W3 control head does not have an interface for VIPs on the control head itself, the radio and the W3 interconnect board must work together to provide VIP OUT at the back of the radio (Figure 2-4). The driving transistors (for the ON/OFF relay control) are located on the W3 interconnect board. Therefore, the microprocessor on the main board uses one set of lines to interface with the interconnect board's transistors and a second set of return lines, which travel back to the main board and pass through to the back of the radio. Also, by using a Y-split cable HKN6096, VIP OUT also can be accessed at its 15-pin connector. However, the voltage levels are slightly lower since the VIP SWB+ of the interconnect board is different from the SWB+ of the radio.

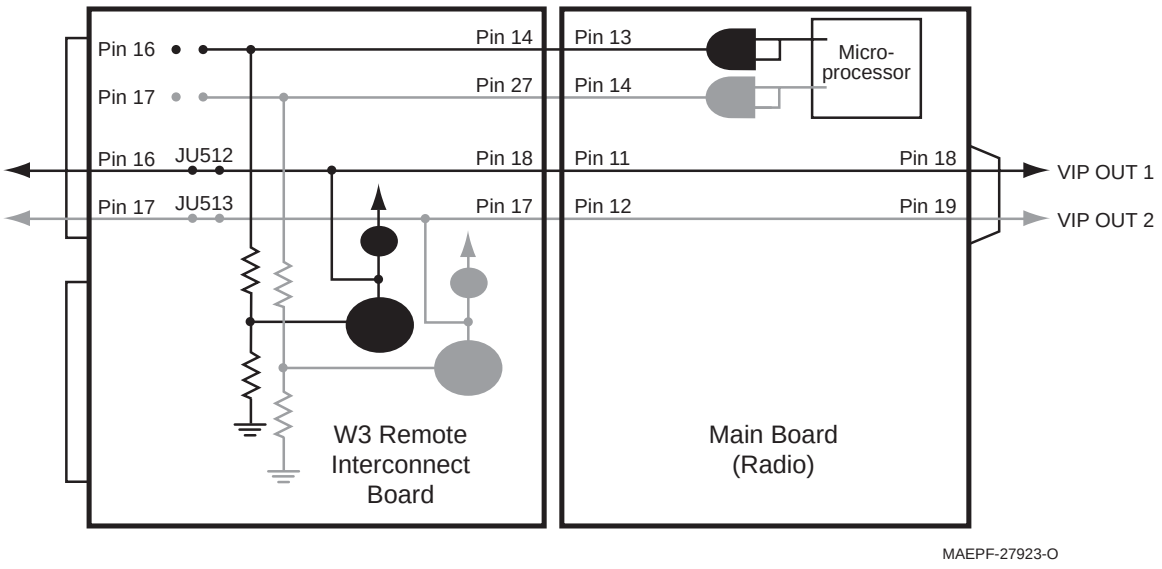

Figure 2-4. VIP Remote-Mount W3 Control-Head Configuration

2.3.2.4 Remote-Mount plus DEK Configuration

Another remote-mount configuration possibility is the addition of up to three Direct Entry Keypad (DEK) boxes (Figure 2-5 on page 2-5). A DEK is an accessory that is used with a mobile radio to provide extra buttons, indicators, and VIPs to the user. Just as the VIP output pins moved from the rear of the radio to the rear of the control head, the VIP pins also move from the back of the control head to the back of the DEK. The benefit of using a DEK box is that you gain three additional VIP OUT and VIP IN pins for each DEK added. The first DEK box provides the original three VIP OUT and three VIP IN pins. The next DEK provides an additional three VIP OUT and three VIP IN pins. A final DEK box provides an additional three VIP OUT and three VIP IN pins for a total of nine VIP OUT and nine VIP IN pins.

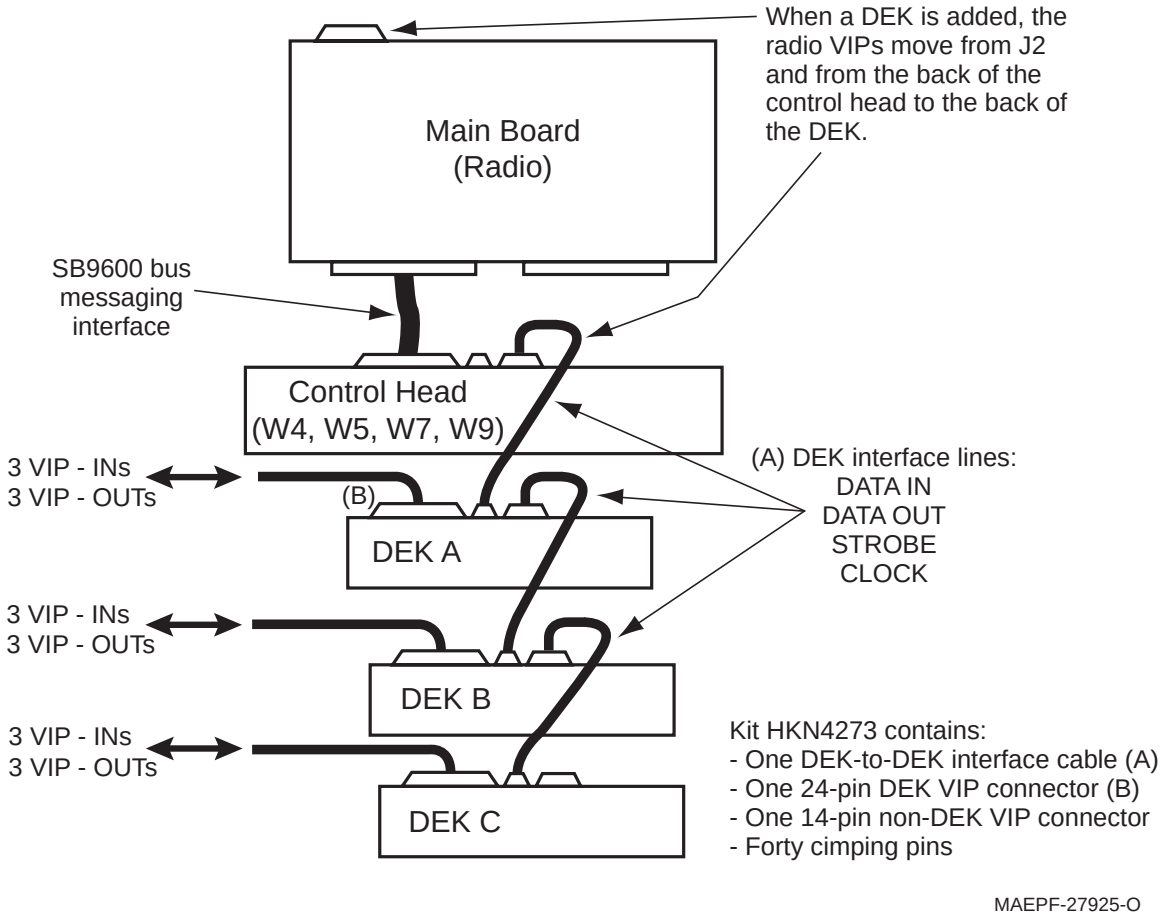

Figure 2-5. VIP Remote-Mount Plus DEK Configuration

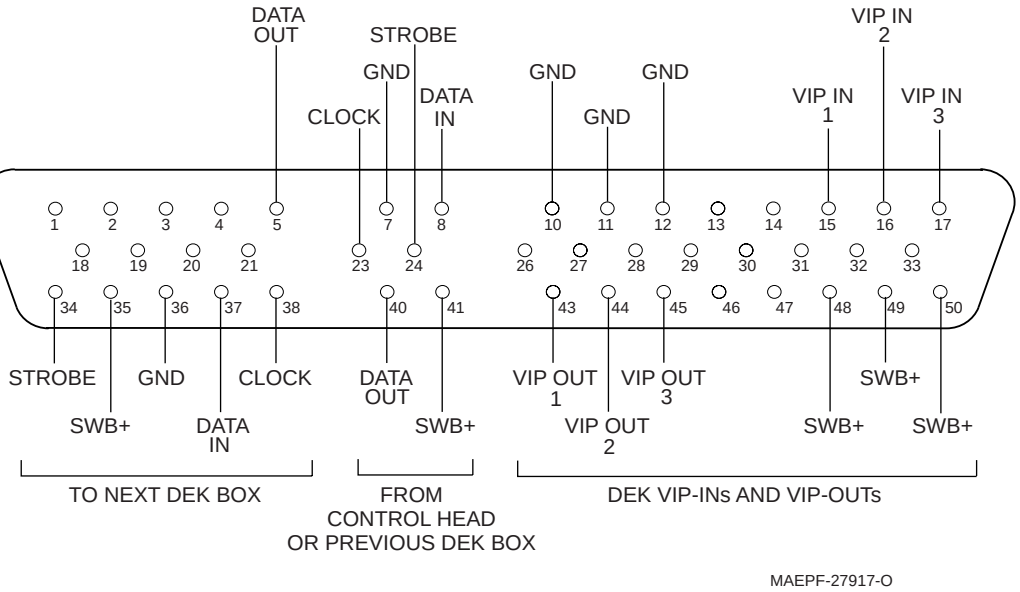

Figure 2-6. VIP Remote-Mount Plus DEK Pin-Outs (Male)

2.3.2.5 VIP Output Connections:

There are three VIP outputs that are used for the W9 control head and two VIP outputs for the W3, W4, W5, and W7 control heads. The VIP outputs are normally at SWB+ levels and are driven low by logic within the control head for both the dash- and remote-mount configurations. Field programming of the radio can define the functions of these pins. The output transistors that drive the VIP outputs can sink 300 mA of current and are primarily used to control external relays. These relays should be connected between the respective VIP output pin and switched B+.

VIP outputs are controlled by SB9600 Update_Indicator messages. Therefore, multiple indicators and their status information can be sent with a single message.

The relay can be normally ON or normally OFF depending on the configuration of the VIP outputs. The CPS can be used to program the function of these VIP outputs in the radio.

The following are typical applications currently supported with ASTRO products:

- Horn relay
- Light relay
- Siren horn transfer

2.3.2.6 VIP Input Connections:

There are three VIP inputs that accept inputs from switches. VIP input messages are sent via the SB9600 pins as SB9600 BUTCTL messages. One side of the switch connects to ground while the other side connects to a buffered input to the control head. The switch can be normally closed or normally open depending on the configuration of the VIP inputs. The CPS can be used to program the function of these VIP inputs in the radio.

The following are typical applications currently supported in ASTRO products:

- Siren horn ring
- Auxiliary siren

Table 2-1. Control-Head VIP Locations

Type	Configur -ation	Power Level	VIP Location	Number of VIP Inputs	Number of VIP Outputs
W3	Remote	Midpower	J3-3 and J3-12 Remote Mount Accessory Cable HKN6096	None	2
W3	Dash	Midpower	J2-18 and J2-19 Rear Accessory Connector	None	2
W4	Dash	Midpower	J2-18 and J2-19 Rear Accessory Connector	None	2
W5	Dash	Midpower	J2-18 and J2-19 Rear Accessory Connector	None	2
W7	Dash	Midpower	J2-18 and J2-19 Rear Accessory Connector	None	2

For the remote configuration of W4, 5, 7 and 9 control heads, refer to sections 3.1.2 and 3.2.1 of the Installation Manual, 6881096C72.

2.3.2.7 DEK Interface With Radio: Remote-Mount (W4, W5, W7, W9)

A maximum of three DEKs can be daisy chained to a single mobile radio. DEKs are *only* used with the W4, W5, W7, and W9 control heads when they are remotely mounted on the radio. DEKs are *not* used with *any* dash-mount control heads, including W4, W5, W7, or W9. The W3 control head does not support DEK, except in a special siren cabling configuration where the DEK 6-pin cable splits off the SIREN cable and plugs into the back of a DEK box.

The VIP lines in the control head are used to connect a DEK. There are four lines that are needed to communicate with the DEK: DATA IN, DATA OUT, STROBE, and CLOCK. These lines are shared with the VIP lines in the control head (see Table 2-1 on page 2-6) and, as a result, the control head loses its VIP lines when connected to a DEK. However, each DEK has its own VIP lines (three VIP IN and three VIP OUT lines) that can be used.

Each DEK box is essentially a shift register consisting of eight buttons/indicators together with the VIP lines. A raw, 48-bit stream of data from the control head is clocked into the first DEK box that is directly connected to it. This DEK box only shifts the bits forward to DEK B, which, in turn, forwards the bits to DEK C. Thus, bit 0 leaving the control head is actually stored as the last bit of DEK C. The full 48 bits is always clocked in/out regardless of the number of DEKs connected. The software is able to determine how many DEKs are actually connected by checking the "DEK present" bit for each DEK. The VIPs provided by each DEK box can then be used for driving external circuitry.

2.3.2.7.1 DATA IN

DATA IN consists of data entering from either the control head or another DEK. DATA IN is a raw bit stream fed into the DEK, which, in turn, essentially being a shift register, moves the data forward to the next DEK. DATA IN is a 48-bit stream that consists of indicator data (0 = off, 1 = illuminated) and VIP output data.

2.3.2.7.2 DATA OUT

DATA OUT consists of data leaving the DEK and either entering a control head or another DEK. DATA OUT is a 48-bit stream that consists of button data (0 = pressed, 1 = released), VIP input data, and DEK present.

2.3.2.7.3 STROBE

The STROBE line is used to latch the data contained in the shift registers inside the DEK box. This line is used to inform the DEK that the data contained in its shift registers is now valid.

2.3.2.7.4 CLOCK

The CLOCK line is used to shift data in and out through the shift registers located in the DEK boxes.

2.3.3 Power Supplies

The +5-V supply is a three-terminal regulator IC to regulate the 12 V SWB+ down for the digital logic hardware.

2.3.4 Ignition Sense Circuits

A transistor senses the vehicle ignition’s state, disabling the radio when the ignition is off. For negative-ground systems, the orange lead is typically connected to the fuse box (+12 V).

2.4 Receiver Section

This section discusses the receiver section components and basic operation for each band.

2.4.1 VHF Band Radios

The VHF (136–174 MHz) receiver consists of a front-end and a back-end sections.

2.4.1.1 Front-End Section

The primary function of the receiver front-end is to optimize image rejection and selectivity while providing the first conversion. The front-end uses discreet filters and LNAs. The first filter reduces the IF spur, image frequency response and limits some of the out-of-band interference. The second filter following the second low-noise amplifier (LNA) provides additional image rejection and half IF spur.

The receiver front-end signal is fed to the monolithic mixer IC where it is down converted to an IF of 109.65 MHz. The mixer is driven by the receiver injection buffer that provides 20 dBm to the mixer. The VCO performs high side injection for the VHF band. The design maintains temperature stability, low insertion loss, and high out-of-band rejection.

2.4.1.2 Back-End Section

The crystal filters provide IF selectivity and out-of-band signal protection to the back-end IC. Two 2-pole crystal filters centered at 109.65 MHz that are isolated from one another by a stable, high-gain low noise amplifier are used to meet the receiver specifications for gain, close-in intermodulation rejection, adjacent-channel selectivity, and second-image rejection.

The output of the IF circuit is fed directly to the Abacus III digital back-end IC. The ABACUS III is an IC with a variable-bandwidth bandpass Sigma-Delta architecture. It is capable of down-converting analog, as well as digital, RF protocols into a baseband signal transmitted on the Synchronous Serial Interface (SSI) bus. The ABACUS III IC converts the 109.65 MHz signal from the IF section down to 2.25 MHz using a second LO frequency of 107.4 MHz or 111.9 MHz. The second LO VCO is tuned to 107.4 MHz (low side), but can be modified to 75.6 MHz (high side injection) depends on known spurious interference related to the programmed received frequency.

2.4.2 UHF Range 1/UHF Range 2 Band Radios

The UHF Range 1 (380–470 MHz)/UHF Range 2 (450–520 MHz) receiver consists of a front-end section and a back-end section.

2.4.2.1 Front-End Section

The receiver front-end consists of a switchable high pass filter and LNA, a preselector, a switchable attenuator, a second switchable low noise amplifier (always in for UHF Range 2), image filter, mixer, and injection amplifier. The preselector filter is varactor-tuned and is aligned at the factory. The radio tuner software can also be used to check and re-align the preselector. The switchable stage provides AGC capability.

The signal from the preselector is amplified by the low noise amplifier, then filtered by the image filter before it is sent to the mixer. The mixer uses the LO signal, amplified by the injection amplifier, to convert the RF signal to IF frequency of 109.65 MHz. This signal is then sent to the IF and back-end circuits.

2.4.2.2 Intermediate Frequency and Back-End

The Intermediate Frequency (IF) consists of a crystal filter, amplifier, a second crystal filter, and a switchable attenuator. This provides selectivity at the IF while attenuating out-of-band signals and protecting the back-end (BE) IC.

The back-end is primarily the ABACUS III digital IC. The ABACUS III IC uses a variable-bandwidth bandpass sigma-delta architecture. It is capable of down-converting analog as well as digital RF protocols into a baseband signal, which is then transmitted over the Synchronous Serial Interface (SSI) bus to the DSP and microprocessor.

2.4.3 700–800 MHz Band Radios

The 700–800 MHz receiver consists of a front-end section and a back-end section.

2.4.3.1 Front-End Section

The primary function of the receiver front-end is to optimize image rejection and selectivity while providing the first conversion. The front-end uses ceramic-filter technology and includes a wideband, monolithic amplifier. The first filter is a dual-switched filter that reduces the image frequency response and limits some of the out-of-band interference. The second filter following the monolithic low-noise amplifier (LNA) provides additional image rejection.

The receiver front-end signal is fed to the monolithic mixer IC where it is down converted to an IF of 73.35 MHz. The mixer is designed to provide low conversion loss and high intermodulation performance. The mixer is driven by the receiver injection buffer, a two-stage discrete IC design used with the receiver VCO to efficiently drive the mixer over a wide temperature range with minimum power variation. The injection buffer provides 15 dBm to the mixer. The VCO performs low-side injection for the 800 MHz band and high-side Injection for the 700 MHz band. The design maintains temperature stability, low insertion loss, and high out-of-band rejection.

2.4.3.2 Back-End Section

The crystal filters provide IF selectivity and out-of-band signal protection to the back-end IC. Two 2-pole crystal filters centered at 73.35 MHz that are isolated from one another by a stable, moderate-gain amplifier are used to meet the receiver specifications for gain, close-in intermodulation rejection, adjacent-channel selectivity, and second-image rejection.

The output of the IF circuit is fed directly to the ABACUS III digital back-end IC. The ABACUS III is an IC with a variable-bandwidth bandpass Sigma-Delta architecture. It is capable of down-converting analog, as well as digital, RF protocols into a baseband signal transmitted on the Synchronous Serial Interface (SSI) bus. The ABACUS III IC converts the 73.35 MHz signal from the IF section down to 2.25 MHz using a second LO frequency of 71.1 MHz or 75.6 MHz. The second LO VCO is tuned to 71.1 MHz (low side) or 75.6 MHz (high side injection). The choice of frequency depends on known spurious interference related to the programmed received frequency.

2.5 Transmitter Section

This section discusses the transmitter section components and basic operation for each band.

2.5.1 VHF Radios

The VHF (136–174 MHz) transmitter consists of an RF power amplifier (RFPA), output network (ON), and power control. See 2.5.3 700–800 MHz Radios below for an overview of the transmitter sections.

2.5.2 UHF Range 1/UHF Range 2 Radios

The UHF Range 1 (380–470 MHz)/UHF Range 2 (450–520 MHz) transmitter consists of an RF power amplifier (RFPA), output network (ON), and power control. See 2.5.3 700–800 MHz Radios below for an overview of the transmitter sections.

2.5.3 700–800 MHz Radios

The 700–800 MHz transmitter consists of an RF power amplifier (RFPA), output network (ON), and power control.

2.5.3.1 RFPA

The RFPA is a three-stage, discrete-LDMOS transistor amplifier consisting of the following stages: first, driver, and final.

The first stage acts as a variable-gain amplifier and feeds the driver stage, which, in turn, feeds the final stage. All of the stages are matched using transmission lines, capacitors, and inductors. Stage drain biases are supplied via A+ or K9.1V and DRV_9.3V (DRV_9.3V is present for UHF Range 1 and UHF Range 2 only). Stage gate biases are supplied via a digital-to-analog converter (DAC) or the RFPA control voltage.

2.5.3.2 Output Network

The output network (ON) consists on the antenna switch, harmonic filter, and power detector. The antenna switch operates in two modes: RX and TX.

In TX mode, the RFPA final stage is connected to the antenna through the harmonic filter and power detector and is isolated from the RX path.

In RX mode, the antenna is connected to the RX front-end through the power detector and the harmonic filter and is isolated from the TX path. The harmonic filter attenuates harmonics generated by the RFPA when the antenna switch is in TX mode and provides extra selectivity in RX mode.

The power detector senses forward and reverse power and generates a detected voltage proportional to each.

2.5.3.3 Power Control

The forward-power and reverse-power detected voltage is fed back to the power control section where it is added to a DAC voltage determined via power tuning and compared to a reference voltage. A control loop corrects the control voltage adjusting the first stage gain to maintain the reference.

2.5.3.4 Circuit Protection

Final-stage current and temperature as well as radio A+ voltage and RFPA control voltage are sensed. If a fault condition is determined, power is cut back to a level that is safe for the particular conditions.

2.6 Frequency Generation Unit

This section discusses the frequency generation unit (FGU) components and basic operation for each band.

2.6.1 VHF MHz Radios

The VHF (136-174 MHz) frequency generation unit consists of the following:

- Low-voltage fractional-N synthesizer IC
- 16.8 MHz reference oscillator IC
- Two receiver (RX) voltage-controlled oscillators (VCOs)
- Two transmitter (TX) voltage-controlled oscillators (VCOs)
- VCO buffer/amplifier circuits

- Associated circuitry

The reference oscillator IC provides a frequency standard to the Fractional-N synthesizer IC, the ABACUS III digital back-end IC, and the controller section. The synthesizer turns on one of the four VCOs (determined by mode and band of operation) and tunes it to the receiver (RX) local oscillator (LO) or transmitter (TX) carrier frequency.

All four voltage-controlled oscillators (VCOs) employ a discrete Colpitts configuration with a N-channel J-FET transistor. The VCOs tank consists of a varactor diode, coupling capacitor, and a resonator. The varactor changes the oscillator frequency when the DC voltage of the steering line changes. The output of the VCOs is coupled to the second transistor for impedance buffering, and its output is coupled to respective TX/RX buffer amplifiers.

In TX mode, the transmitter VCO output is coupled to a three-stage buffer before being injected into the power amplifier. In RX mode, the receiver VCO output is buffered and amplified with a two-stages. The output of the second-stage transistor is split into two paths. One path feeds back to the synthesizer prescaler; the other path is injected into the third-stage. The output of the third-stage provides the proper signal level for the LO port of the RX front-end mixer.

The superfilter supplies the voltage to the first two stages of the TX buffer and to the first two stages transistor of the RX buffer/amplifier. The voltage for the third stage of the TX buffer is supplied by a keyed 9.1 V source to conserve current drain while the radio is receiving. The third-stage of the RX buffer/amplifier is supplied by a 9.3 V regulator.

2.6.2 UHF Range 1/UHF Range 2 Radios

The UHF Range 1 (380–470 MHz)/UHF Range 2 (450–520 MHz) frequency generation unit consists of the following:

- Low-voltage fractional-N synthesizer IC
- 16.8 MHz reference oscillator IC
- Three receive voltage-controlled oscillators (VCO)
- Two transmit VCOs
- VCO buffer/amplifier circuits
- Associated circuitry

See 2.6.3 700–800 MHz Radios below for an overview of the FGU sections.

2.6.3 700–800 MHz Radios

The 700–800 MHz frequency generation unit consists of the following:

- Low-voltage fractional-N synthesizer IC
- 16.8 MHz reference oscillator IC
- Two voltage-controlled oscillator (VCO) modules (receive and transmit, containing two VCOs each)
- VCO buffer/amplifier circuits
- Associated circuitry

The reference oscillator IC provides a frequency standard to the fractional-N synthesizer IC, the ABACUS III digital back-end IC, and the controller section. The synthesizer turns on one of the four VCOs (determined by mode and band of operation) and tunes it to the receiver (RX) local oscillator (LO) or transmitter (TX) carrier frequency.

The voltage-controlled oscillator (VCO) module employs a Colpitts configuration with two bipolar stages in a common-base, common-collector configuration. The LC tank circuit's capacitive portion consists of a varactor diode, coupling capacitor, and a laser-trimmed capacitor for frequency adjustment. The inductive portion consists of microstrip transmission line resonators for TX VCO and coaxial resonators for RX VCO. Tuning is performed by the module manufacturer and is not field adjustable. The varactor changes the oscillator frequency when the DC voltage of the steering line changes. The output of the common base is coupled to the second transistor for impedance buffering, and its output is coupled to respective TX/RX buffer amplifiers.

In TX mode, the transmitter VCO output is coupled to a three-stage buffer before being injected into the power amplifier. In RX mode, the receiver VCO output is buffered and amplified with a two-stage transistor/microwave monolithic IC (MMIC) circuit. The output of the first-stage transistor is split into two paths. One path feeds back to the synthesizer prescaler; the other path is injected into the second-stage MMIC. The output of the MMIC provides the proper signal level for the LO port of the RX front-end mixer.

The superfilter supplies the voltage to the first two stages of the TX buffer and to the first-stage transistor of the RX buffer/amplifier. The voltage for the third stage of the TX buffer is supplied by a keyed 9.1 V source to conserve current drain while the radio is receiving. The second-stage MMIC of the RX buffer/amplifier is supplied by a 9.3 V regulator.

2.7 Controller Section

This section provides an explanation of radio operating modes and an overview of the controller section components and circuits.

2.7.1 Analog Mode of Operation

When the radio is receiving, the signal comes from the antenna/antenna-switch to the front-end receiver. The signal is then filtered, amplified, and mixed with the first local-oscillator signal generated by the voltage-controlled oscillator (VCO). The resulting intermediate frequency (IF) signal is fed to the IF circuitry, where it is again filtered and amplified. This amplified signal is passed to the digital back-end IC, where it is mixed with the second local oscillator to create the second IF at 2.25 MHz. The analog IF is processed by an analog-to-digital (A/D) converter inside the digital back-end IC where it is converted to a digital bit stream and divided down to a baseband signal, producing digital samples. These samples are converted to TTL logic signals and sent to the DSP. The DSP digitally filters and discriminates the signal, decodes the information in the signal, and identifies the appropriate destination for it. For a voice signal, the DSP will route the digital voice data to the coder/decoder (CODEC) for conversion to an analog signal. The CODEC will then present the signal to the audio power amplifier, which drives the speaker. For signalling information, the DSP will decode the message and pass it to the microcomputer.

When the radio is transmitting, microphone audio is passed to an adjustable gain circuit, then to the CODEC where the signal is digitized. The CODEC passes digital data to the DSP where pre-emphasis and low-pass (splatter) filtering are done. The DSP sends this signal to the modulation digital-to-analog (D/A) converter where it is reconverted into an analog signal and scaled for application to the voltage-controlled oscillator as a modulation signal. Transmitted signalling information is accepted by the DSP from the microcomputer, coded appropriately, and passed to the modulation D/A converter, which handles it the same as a voice signal. Modulation information is passed to the synthesizer along the modulation line. A modulated carrier is provided to the power amplifier (PA), which transmits the signal under dynamic power control.

2.7.2 Digital (ASTRO) Mode of Operation

In the ASTRO mode (digital mode) of operation, the transmitted or received signal is limited to a discrete set of deviation levels, instead of continuously varying. The receiver handles an ASTRO-mode signal identically to an analog-mode signal up to the point where the DSP decodes the received data. In the ASTRO receive mode, the DSP uses a specifically defined algorithm to recover information. In the ASTRO transmit mode, microphone audio is processed identically to an analog mode with the exception of the algorithm the DSP uses to encode the information. This algorithm will result in deviation levels that are limited to discrete levels.

2.7.3 Controller Section Circuitry

The controller section consists of the following:

- Voltage regulators
- Data connectivity circuitry (RS-232, USB, and SB9600)
- Daughtercard module, which contains the:
  - Patriot microprocessor IC
  - 64-Mbit (8MB) FLASH IC
  - 8-Mbit (1MB) SRAM IC
- Modulation D/A conversion circuitry
- CODEC audio circuitry
- TX power-control circuitry
- Emergency circuitry
- V.I.P input/output paths
- Secure interconnect board interface
- Front connector interface for control heads and remote-mount interconnect boards (I.B)
- Rear connector for additional accessories
- DC power-in plug

The controller section controls receive/transmit frequencies, the display, and various radio functions using either direct logic control or serial communication to external devices. The connector J0701 provides interface between the encryption module and the controller for encrypting voice messages.

Connector J0402 provides the accessory interface to the outside rear connector while connector J0401 provides the control-head interface.

The controller section executes a stored program located in the FLASH ROM. Data is transferred to and from memory via an RS-232 interface on the microprocessor. The memory location from which data is read, or to which data is written, is selected by the address lines. Besides the host and DSP code, the customer-specific programming features (codeplug) and tuning parameters also are stored in the FLASH ROM. The SRAM is used as scratchpad memory for the microprocessor.

The controller section is powered by SW_B+ coming from the control head, which is regulated down to a 5 V supply. This supply powers the entire controller section and its regulators. The SW_B+ supply is removed from the board when the radio is turned off by the control-head switch.

The microprocessor is powered by a 1.55-V regulator for the microprocessor core and a 2.85-V regulator for the I/O and control lines, while the memory is powered by a 1.85-V regulator. The 2.85-V regulator also supplies almost all of the discrete controller circuitry. These three regulators are all supplied by a switched 5-V regulator, which also provides power for the SB9600 data bus and for interface to certain legacy data and control signals.

The DSP section of microprocessor performs signaling, voice encoding/decoding, audio filtering, microphone gain and tuning, Private-Line/Digital Private Line (PL/DPL) encode, and alert-tone generation. It processes all baseband audio signals, providing pre-emphasis and signaling/filtering of the digital microphone audio data, as well as other transmitted signals. It also performs de-emphasis and decoding of received digital speaker audio and other received signals. The DSP clock frequency is derived from the 16.8 MHz reference oscillator clock input using a phase-locked loop (PLL) inside the Patriot IC. The digital audio bus on the Patriot IC uses an 8 kHz clock, which provides the sampling rate, and a 512 kHz clock, which provides the data rate.

The CODEC performs analog-to-digital and digital-to-analog conversions on audio signals. The DSP controls squelch, deviation, and compensation, and it executes receiver filtering and discrimination.

The interface to the RX back-end IC (ABACUS III IC) consists of a single logic-level data line, a 1.2 MHz clock line (the discriminator data bit rate) and a 20 kHz frame-sync line (the discriminator data sample rate). These clocks are generated by the ABACUS III IC and provided to the Patriot IC.

The interface to the TX modulation/DAC consists of a single logic-level data line, a 2.4 MHz clock line (the modulation data bit rate), and a 48 kHz clock line (the modulation data sample rate). These clocks are generated by the Urchin IC and provided to the Patriot IC.

Other functions provided by the controller include SB9600 communication, IC programming, and TX power control. The SB9600 bus is used to communicate to legacy control heads and accessories. IC programming is performed via the SPI bus for ICs including the ABACUS III, LV Frac-N, A/D, D/A, and volume attenuator. The power-control circuitry receives power set and limit inputs from the D/A IC and feedback from the RF power amplifier (RFPA). Based on these inputs, the circuit produces a control voltage to maintain a fixed RF power level to the antenna.

The controller also provides detection of the On/Off and reset inputs. The reset circuits consist of the regulator power-on reset circuit, low SW_B+ voltage-detector circuit, an ignition detection circuit, an emergency detection circuit, and the external-bus system reset. The reset circuits allow the microcomputer to recover from an unstable situation; for example, no battery on the radio, battery voltage too high or too low, and remote devices on the external bus not communicating. Communication using RS-232 protocol is provided to the rear accessory connector (J2).

Chapter 3 Theory of Operation

3.1 Main Board

This section provides a detailed circuit description of the XTL 5000 radio main board for VHF/UHF Range 1/UHF Range 2/700–800 MHz models. The main board contains the following major sections:

- Radio Power (page 3-12)
- Receiver Front-End (page 3-13)
- Receiver Back-End (page 3-20)
- Transmitter (page 3-26)
- Frequency Generation Unit (page 3-45)
- Controller (page 3-62)

When reading the theory of operation, refer to your appropriate schematic and component location diagrams located in “Chapter 7. Schematics, Component Location Diagrams, and Parts Lists”. This detailed Theory of Operation will help isolate the problem. However, first use the *ASTRO Digital XTL 5000 VHF/UHF Range 1/UHF Range 2/700–800 MHz Mobile Radio Basic Service Manual* (6881096C73) to troubleshoot the problem to a particular board.

3.2 Main Board Major Sections

This section contains the main board layouts for each radio frequency band.

3.2.1 VHF (136–174 MHz) Band

The illustrations (Figure 3-1 on page 3-2 to Figure 3-4 on page 3-5) and their accompanying tables (Table 3-1 on page 3-2 to Table 3-4 on page 3-5) identify the location of the major sections of the main board.

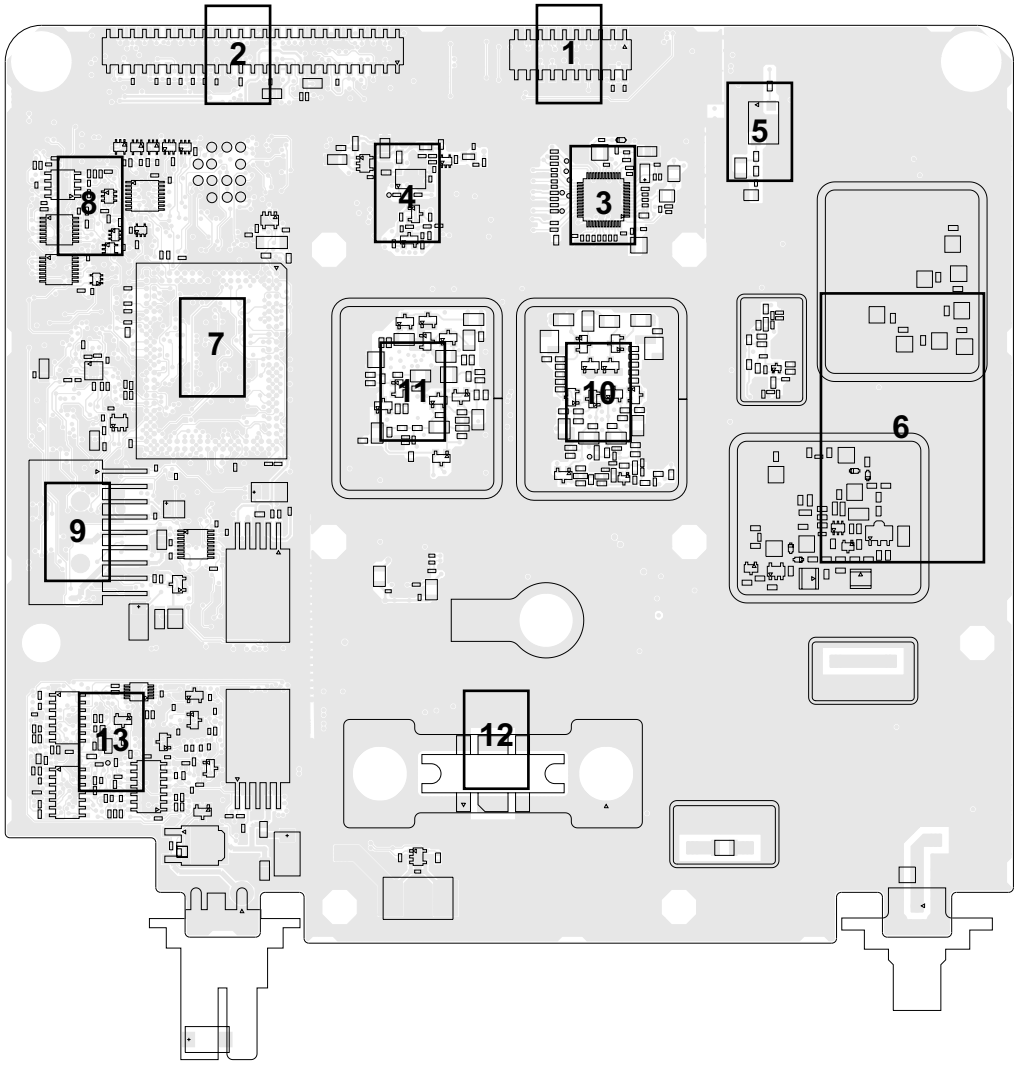

Figure 3-1. XTL 5000 Main Board Sections (VHF Mid Power)—Side 1

Table 3-1. XTL 5000 Main Board Sections (VHF Mid Power)—Side 1

1	Secure Connector (J0501)	8	Controller Section
2	Front Connector (J0401)	9	Audio Power Amplifier (PA)
3	RX Back-End (ABACUS III)	10	RX VCO
4	16.8 MHz Reference Oscillator	11	TX VCO
5	IF Filter	12	TX PA
6	RX Front-End	13	TX Power Control
7	Daughtercard		

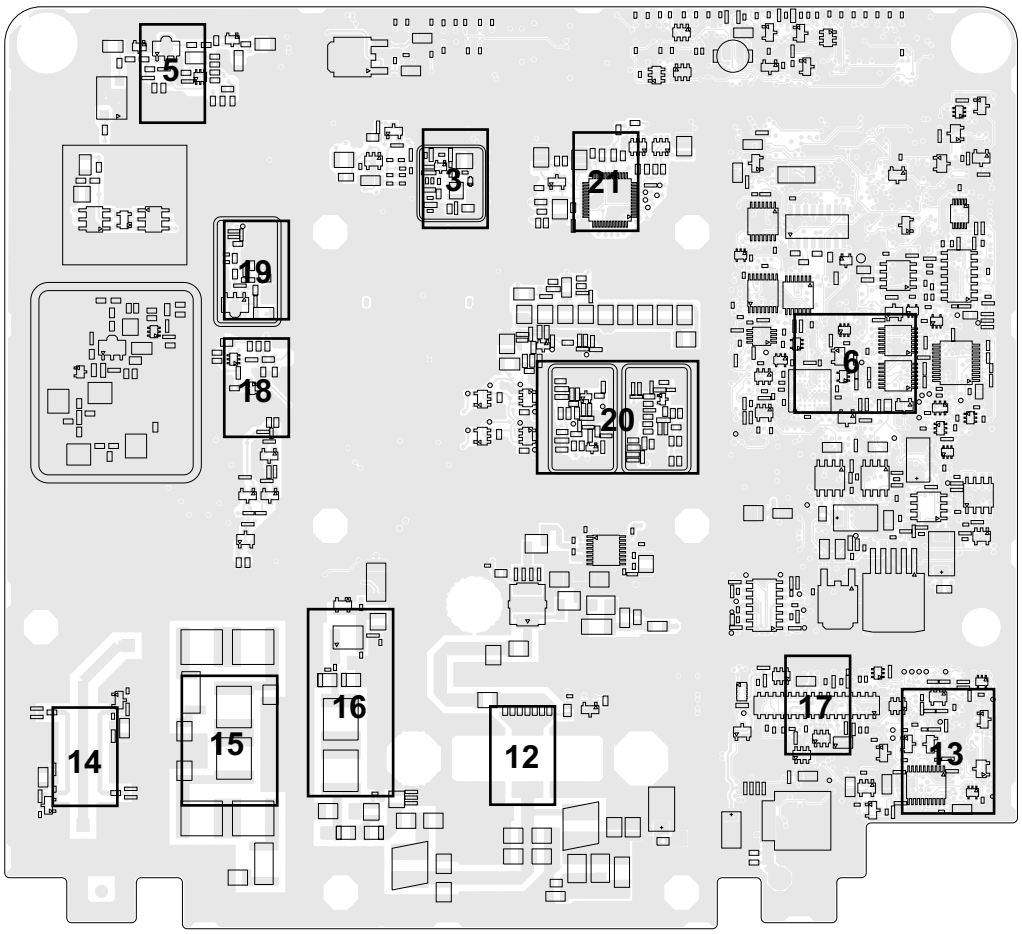

Figure 3-2. XTL 5000 Main Board Sections (VHF Mid Power)—Side 2

Table 3-2. XTL 5000 Main Board Sections (VHF Mid Power)—Side 2

3	RX Back-End	16	Antenna Switch
5	IF Filter	17	Rear Connector (J0402)
6	Controller Section	18	RX Front-End Biasing
12	TX PA	19	RX VCO Injection Stage
13	TX Power Control	20	TX VCO Injection Stage
14	Power Detector	21	FGU (Synthesizer)
15	Harmonic Filter		

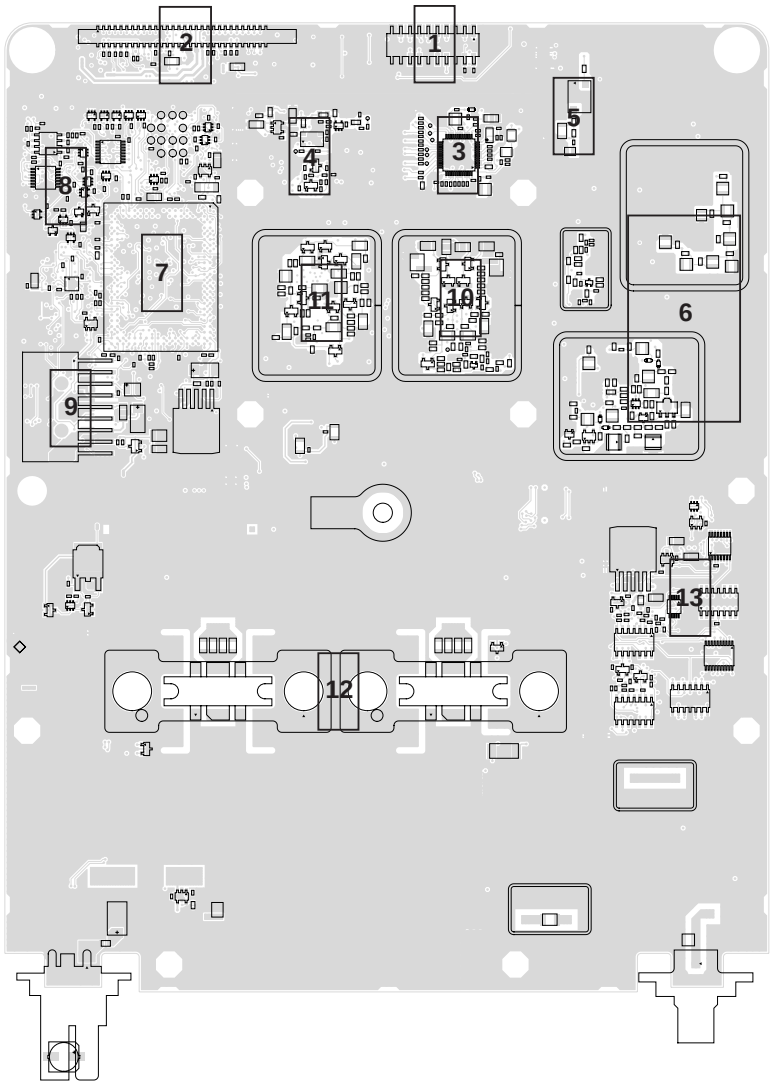

Figure 3-3. XTL 5000 Main Board Sections (VHF High Power)—Side 1

Table 3-3. XTL 5000 Main Board Sections (VHF High Power)—Side 1

1	Secure Connector (J0501)	8	Controller Section
2	Front Connector (J0401)	9	Audio Power Amplifier (PA)
3	RX Back-End (ABACUS III)	10	RX VCO
4	16.8 MHz Reference Oscillator	11	TX VCO
5	IF Filter	12	TX PA
6	RX Front-End	13	TX Power Control
7	Daughtercard		

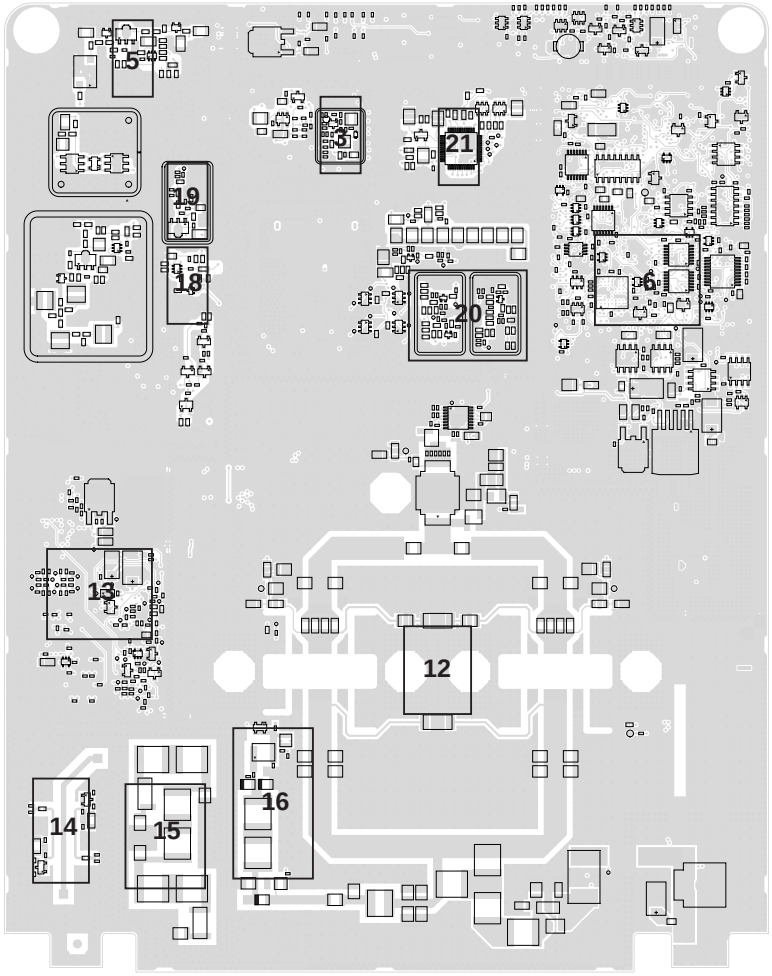

Figure 3-4. XTL 5000 Main Board Sections (VHF High Power)—Side 2

Table 3-4. XTL 5000 Main Board Sections (VHF High Power)—Side 2

3	RX Back-End	16	Antenna Switch
5	IF Filter	17	Rear Connector (J0402)
6	Controller Section	18	RX Front-End Biasing
12	TX PA	19	RX VCO Injection Stage
13	TX Power Control	20	TX VCO Injection Stage
14	Power Detector	21	FGU (Synthesizer)
15	Harmonic Filter		

3.2.2 UHF Range 1 (380-470 MHz) and UHF Range 2 (450-520 MHz) Band

The illustrations (Figure 3-5 on page 3-6 to Figure 3-8 on page 3-9) and their accompanying tables (Table 3-5 on page 3-6 and Table 3-8 on page 3-9) identify the location of the major sections of the main board.

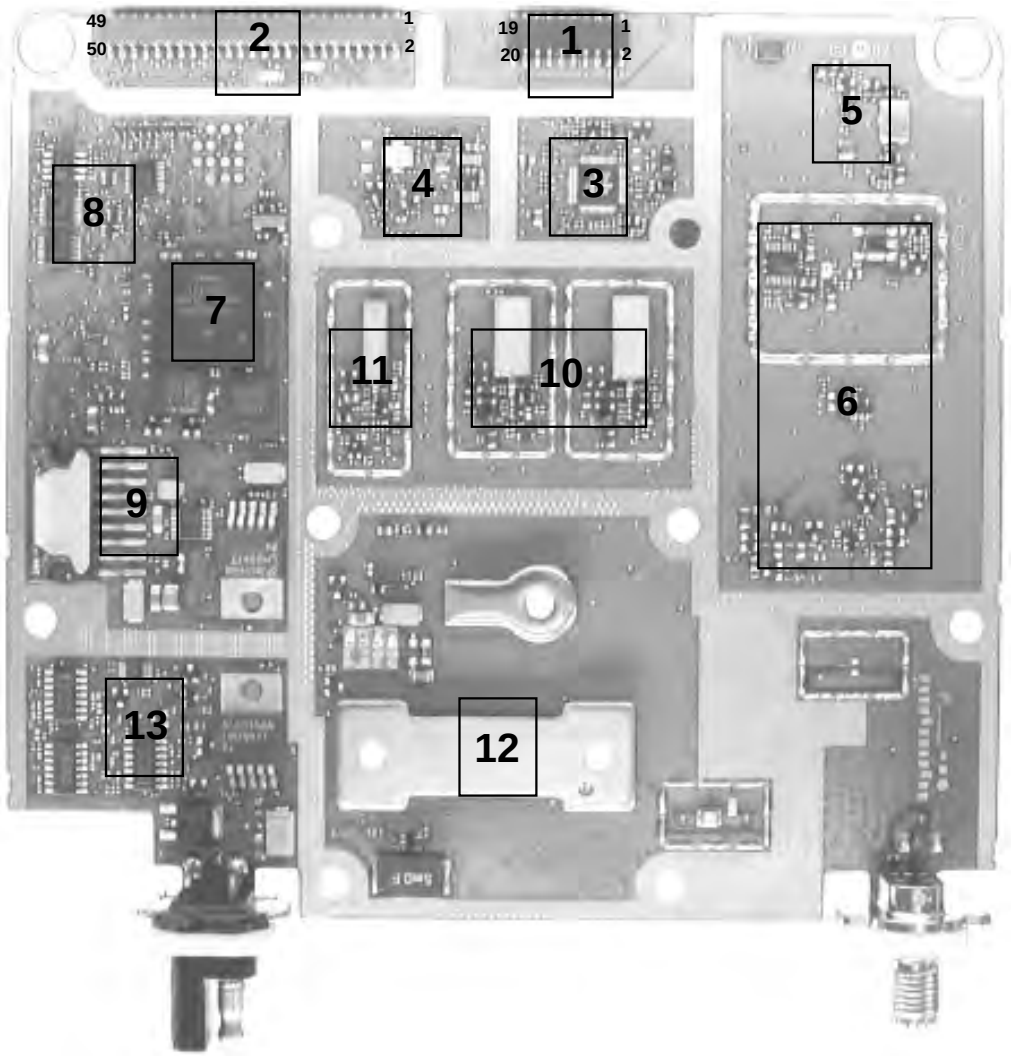

Figure 3-5. XTL 5000 Main Board Sections (UHF Range 1 Mid Power and UHF Range 2)—Side 1

Table 3-5. XTL 5000 Main Board Sections (UHF Range 1 Mid Power and UHF Range 2)—Side 1

1	Secure Connector (J0501)	8	Controller Section
2	Front Connector (J0401)	9	Audio Power Amplifier (PA)
3	RX Back-End (ABACUS III)	10	RX VCO
4	16.8 MHz Reference Oscillator	11	TX VCO
5	IF Filter	12	TX PA
6	RX Front-End	13	TX Power Control
7	Daughtercard		

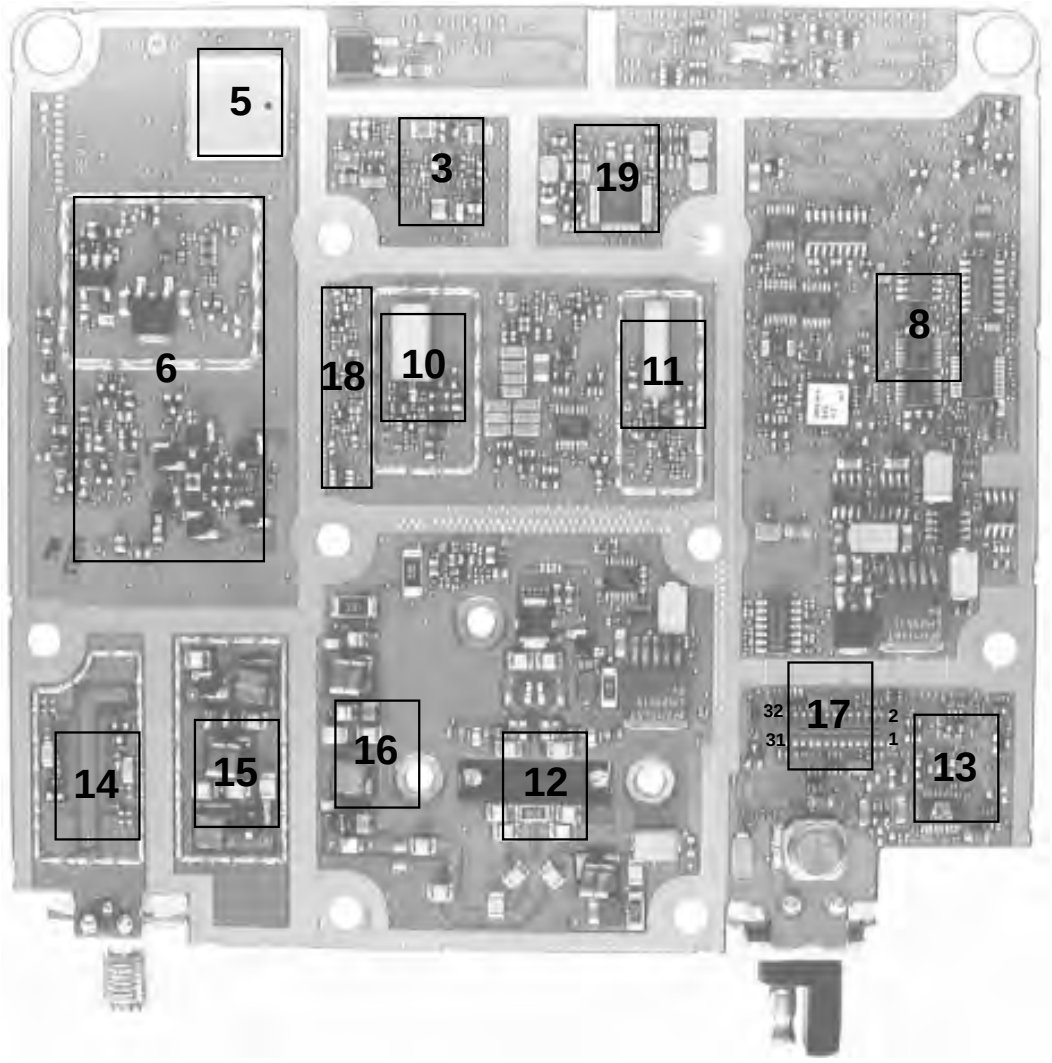

Figure 3-6. XTL 5000 Main Board Sections (UHF Range 1 Mid Power and UHF Range 2)—Side 2

Table 3-6. XTL 5000 Main Board Sections (UHF Range 1 Mid Power and UHF Range 2)—Side 2

3	RX Back-End	13	TX Power Control
5	IF Filter	14	Power Detector
6	RX Front-End	15	Harmonic Filter
8	Controller Section	16	Antenna Switch
10	RX VCO	17	Rear Connector (J0402)
11	TX VCO	18	RX VCO Injection Stage
12	TX PA	19	FGU (Synthesizer)

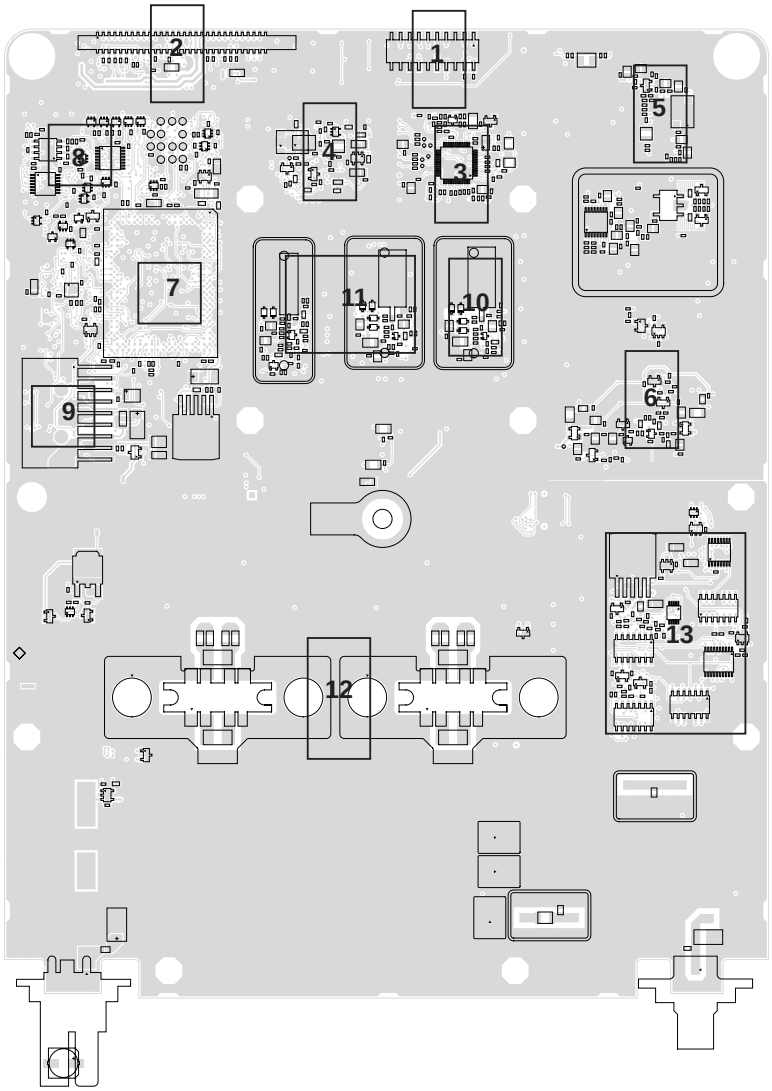

Figure 3-7. XTL 5000 Main Board Sections (UHF Range 1 High Power)—Side 1

Table 3-7. XTL 5000 Main Board Sections (UHF Range 1 High Power)—Side 1

1	Secure Connector (J0501)	8	Controller Section
2	Front Connector (J0401)	9	Audio Power Amplifier (PA)
3	RX Back-End (ABACUS III)	10	RX VCO
4	16.8 MHz Reference Oscillator	11	TX VCO
5	IF Filter	12	TX PA
6	RX Front-End	13	TX Power Control
7	Daughtercard		

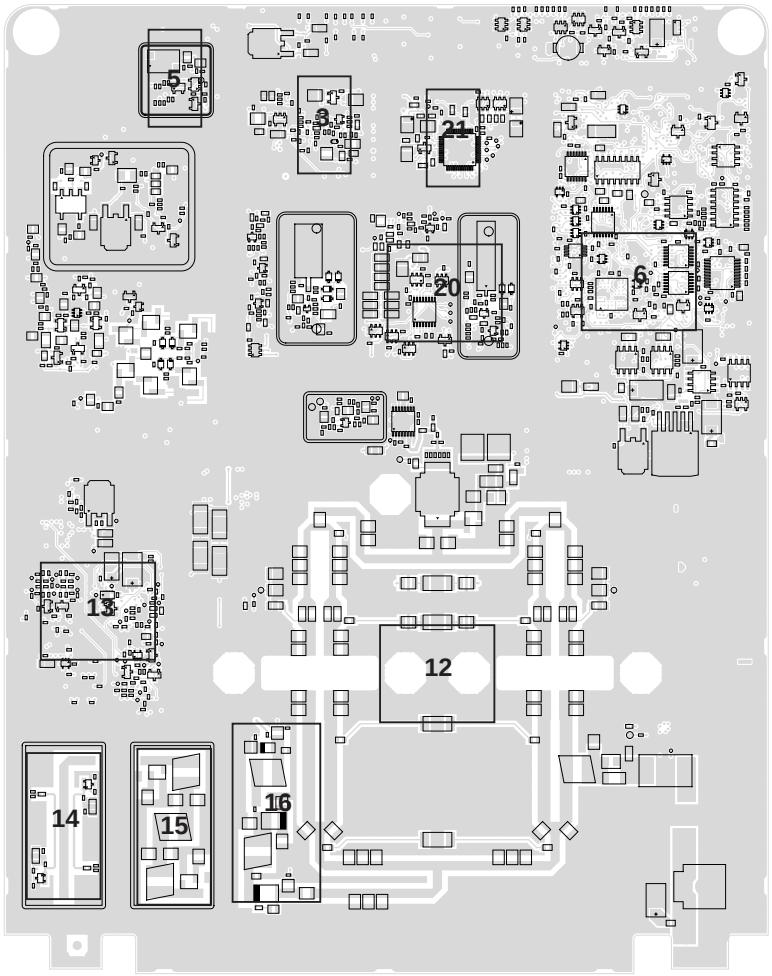

Figure 3-8. XTL 5000 Main Board Sections (UHF Range 1 High Power)—Side 2

Table 3-8. XTL 5000 Main Board Sections (UHF Range 1 High Power)—Side 2

3	RX Back-End	13	TX Power Control
5	IF Filter	14	Power Detector
6	RX Front-End	15	Harmonic Filter
8	Controller Section	16	Antenna Switch
10	RX VCO	17	Rear Connector (J0402)
11	TX VCO	18	RX VCO Injection Stage
12	TX PA	19	FGU (Synthesizer)

3.2.3 700–800 MHz Band

The illustrations (Figure 3-9 and Figure 3-10 on page 3-11) and their accompanying tables (Table 3-9 and Table 3-10 on page 3-11) identify the location of the major sections of the main board.

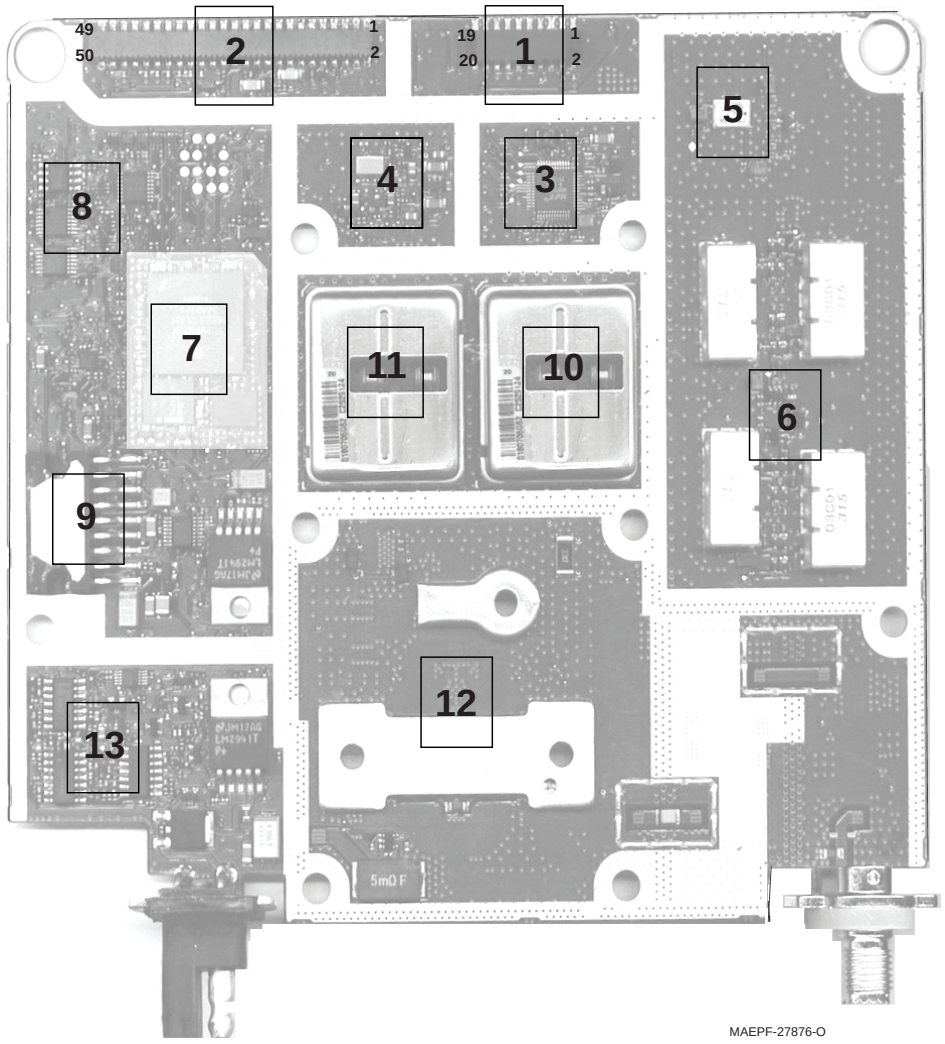

Figure 3-9. XTL 5000 Main Board Sections (700–800 MHz)—Side 1

Table 3-9. XTL 5000 Main Board Sections (700–800 MHz)—Side 1

1	Secure Connector (J0501)	8	Controller Section
2	Front Connector (J0401)	9	Audio Power Amplifier (PA)
3	RX Back-End (ABACUS III)	10	RX VCO
4	16.8 MHz Reference Oscillator	11	TX VCO
5	IF Filter	12	TX PA
6	RX Front-End	13	TX Power Control
7	Daughtercard		

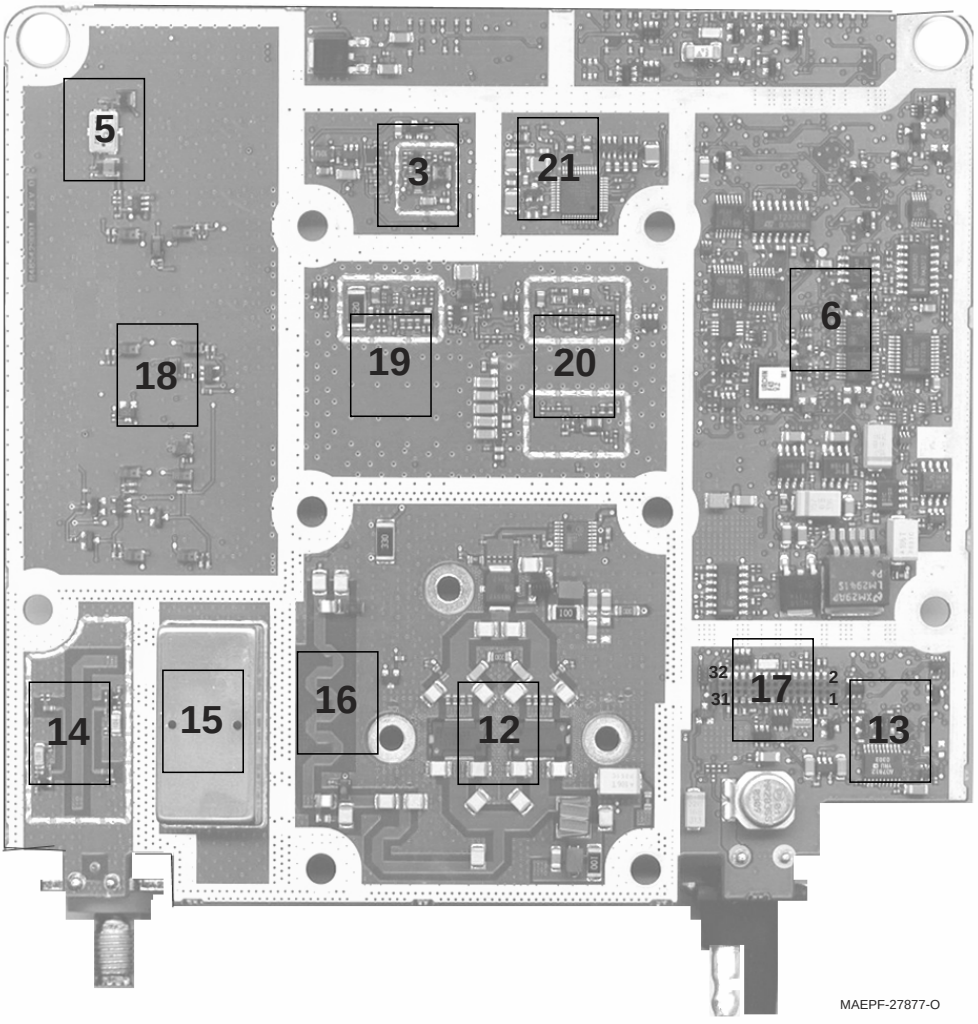

Figure 3-10. XTL 5000 Main Board Sections (700–800 MHz)—Side 2

Table 3-10. XTL 5000 Main Board Sections (700–800 MHz)—Side 2

3	RX Back-End	16	Antenna Switch
5	IF Filter	17	Rear Connector (J0402)
6	Controller Section	18	RX Front-End Biasing
12	TX PA	19	RX VCO Injection Stage
13	TX Power Control	20	TX VCO Injection Stage
14	Power Detector	21	FGU (Synthesizer)
15	Harmonic Filter		

3.3 Radio Power Distribution

This section provides information on DC power distribution in XTL 5000 radios. In the XTL 5000 radio, power is distributed to three boards: the main board, control head, and secure interface board.

Power for the radio is supplied by the vehicle's 12-V battery. When using a desktop adapter unit, an external DC power supply can be connected to replace the vehicle's battery source.

A+ (referred to as incoming unswitched battery voltage) enters the radio through the rear RF power amplifier connector (J0950) and is the main entry for DC power. The second path, through J2, pin 25, provides ignition sense to inhibit radio turn-on when the ignition switch is off.

When the control-head On/Off button is turned on, the three 9.3-V regulators power on the controller section, the RX/frequency generation unit (FGU) section, and the TX section. See Figure 3-11 for the UHF Range 1 and UHF Range 2 bands or Figure 3-12 on page 3-13 for the VHF and 700-800 MHz bands.

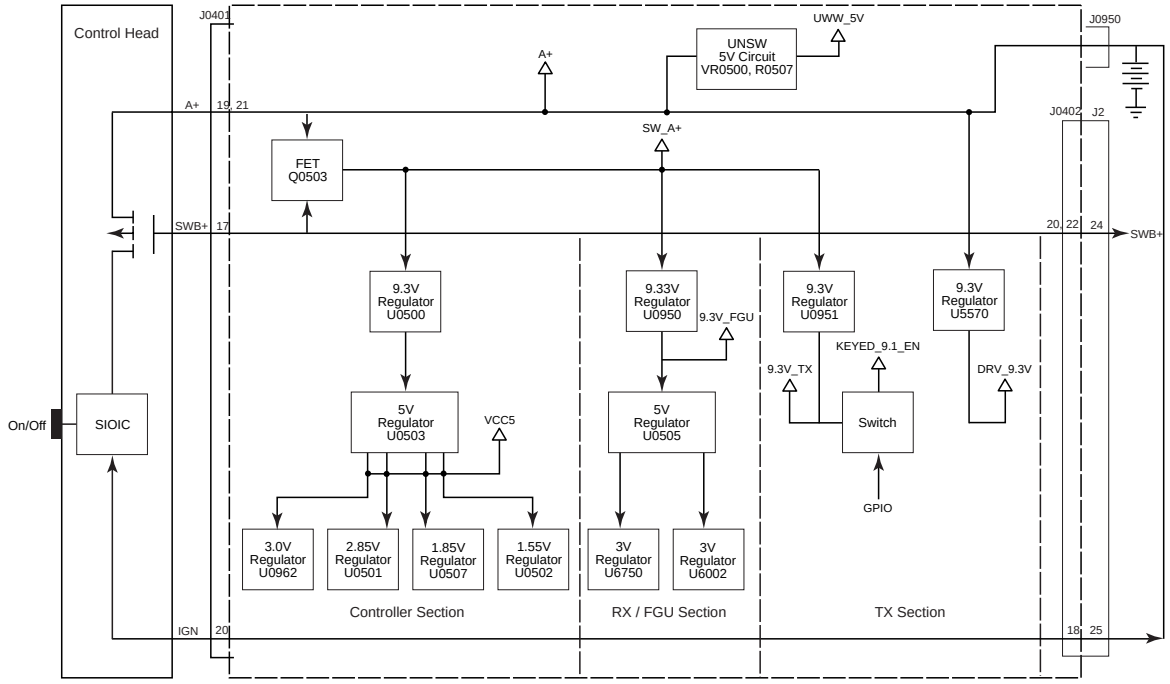

Figure 3-11. DC Voltage Routing Block Diagram (UHF Range 1 and UHF Range 2)

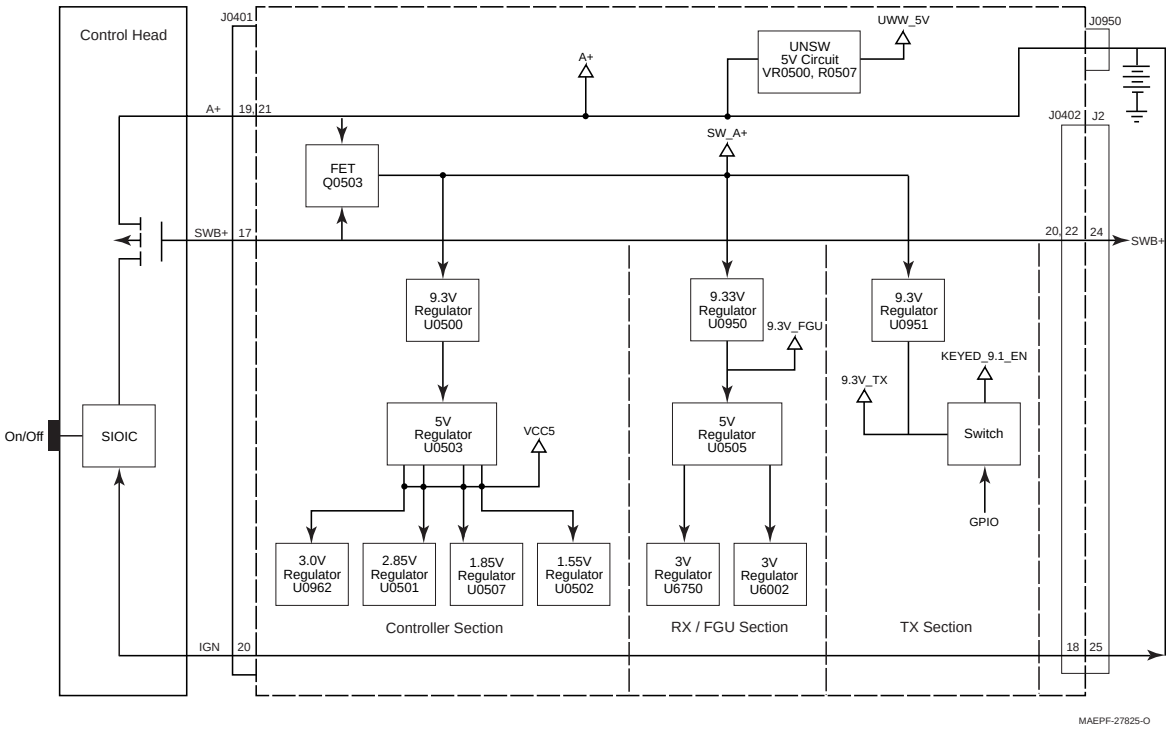

Figure 3-12. DC Voltage Routing Block Diagram (VHF and 700–800 MHz)

The 9.3 V and the A+ voltage are the main DC power for the RF section. The 9.1 V (referred to as “keyed 9.1 V”) is controlled by the VOCON board through P501, pin 45. This DC voltage enables the transmitter’s RF power amplifier when the VOCON board senses a lock detect from the synthesizer.

3.4 Receiver Front-End

This section provides a detailed circuit description of receiver front-end (RXFE). When reading the Theory of Operation, refer to your appropriate schematic and component location diagrams located in “Chapter 7. Schematics, Component Location Diagrams, and Parts Lists”. This detailed theory of operation will help isolate the problem to a particular component.

3.4.1 VHF (136–174 MHz) Band

The receiver circuits primary duties are to detect, filter, amplify, and demodulate RF signals in the presence of strong interfering noise and unintended signals. The receiver is broken down into the following blocks (Figure 3-13 on page 3-14):

- Front-end, which includes:
  - 15 dB step attenuator
  - PIN diode switches
  - Three discrete filters
  - Two low-noise amplifiers
  - Mixer
- Back-end, which includes:
  - Two crystal filters

- Low-noise IF amplifier
- ABACUS III digital back-end IC

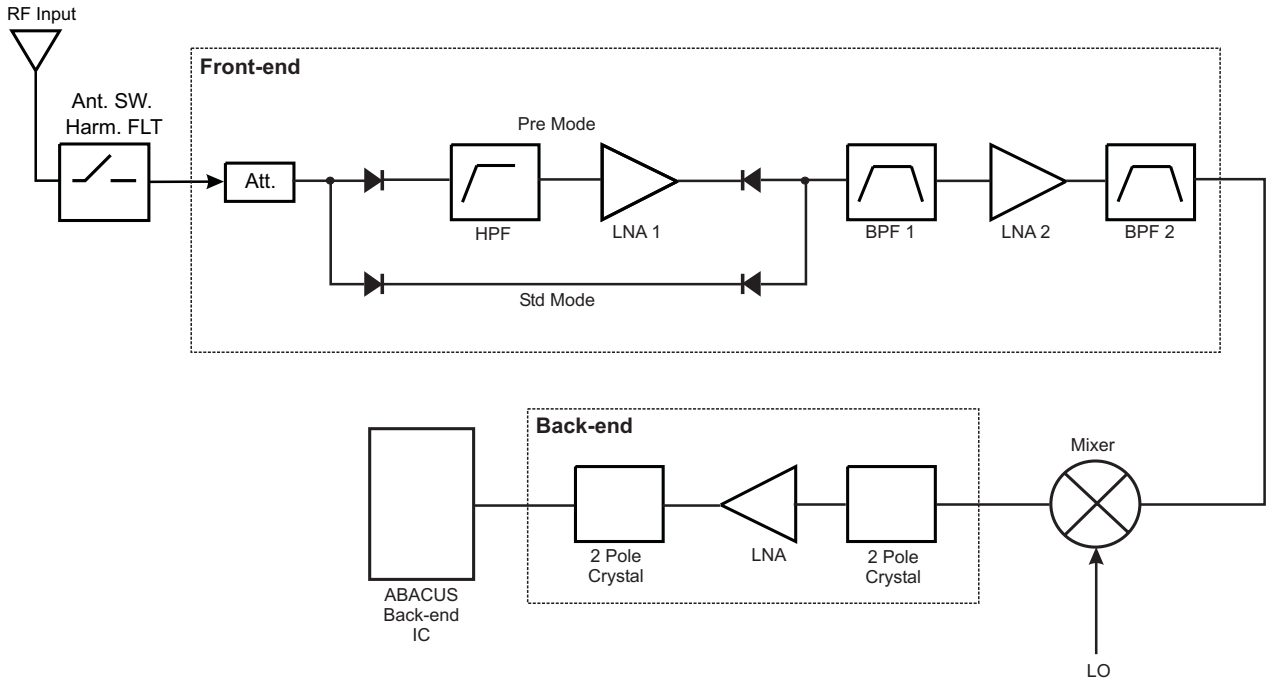

Figure 3-13. Receiver Block Diagram (VHF)

3.4.1.1 15 dB Step Attenuator (U3250)

The 15 dB step attenuator provides protection from strong on-channel signals and interferences.

3.4.1.2 PIN Diode Switches

The VHF front end operates in two modes: Standard mode and Preamp mode. The PIN diode switches select between the two modes. In standard mode the intermodulation performance is improved by bypassing the first HPF and LNA. Preamp mode is characterized by higher sensitivity.

3.4.1.3 Preselector Filters

The front-end operates in the 136-174 MHz band. The front-end filters primary function is to provide protection against out-of-band spurious responses such as image, IF, half-IF, etc. while providing flat, low-loss response in the receive band. The front-end uses discrete LC filter technology. The first filter is a high-pass filter that protects the first LNA from strong out-of-band signals at frequencies which are below the receive band and is used in preamp mode only. The second and third filters are band-pass filters that provide additional out-of-band spurious rejection.

3.4.1.4 Low-Noise Amplifiers (Q3255, Q3252)

The function of the Low-Noise Amplifiers (LNA) is to amplify the received signal with minimal noise contribution. The first LNA (Q3255) has 10 dB of gain and is activated in Preamp mode only. A clamping diode pair (D3256) located after the High Pass and before the first LNA protects the receiver from strong RF signals by limiting the signal amplitude going into the amplifier. The second LNA (Q3252) has 15 dB of gain. Both LNAs are biased with 9.3V.

3.4.1.5 Mixer (D3258)

The received signal is down-converted by a double-balanced mixer to an Intermediate Frequency (IF) of 109.65 MHz. The mixer is designed to provide low conversion loss and high intermodulation performance. The injection buffer provides a 20 dBm LO signal to the mixer. High-side injection is used.

3.4.2 UHF Range 1 (380–470 MHz) Band

The receiver circuits primary duties are to detect, filter, amplify, and demodulate RF signals in the presence of strong interfering noise and unintended signals. The receiver (see Figure 3-14) is broken down into the following blocks:

- Front-end, which includes:
  - High pass fIlter and first low-noise amplifier (LNA)
  - Preselector filter
  - Switchable 15 dB attenuator
  - Second LNA
  - Image Filter
  - First mixer
- Back-end, which includes:
  - Intermediate Frequency (IF)
  - ABACUS III IC

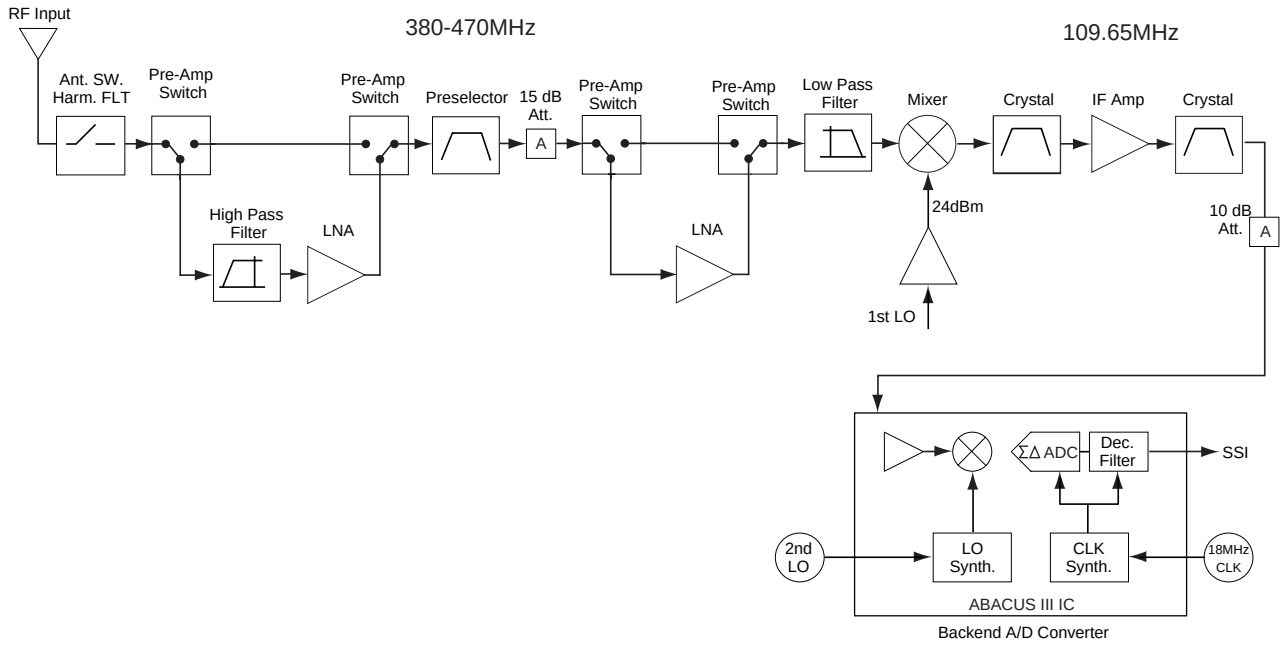

Figure 3-14. Receiver Front-End and Back-End (UHF Range 1)

3.4.2.1 Highpass Filter and First Low-Noise Amplifier

The highpass filter and first low-noise amplifier (LNA) (11 dB gain) can be switched in and out of the signal path by diode switches. When switched into the signal path, the sensitivity of the radio is improved at the cost of degraded intermodulation performance. This can be necessary in fringe areas when strong interference that can lead to intermodulation problems are not present and the desired signal is weak.

The preamplifier version of the radio must be purchased to be able to control this option. If it has not been purchased, the direct path created by the diode switches is the only one available, giving the radio standard model performance with enhanced intermodulation rejection. Purchasing the preamplifier option allows the user to select either mode with the CPS.

3.4.2.2 Preselector Filter

The front-end operates in the 380 to 470 MHz band. The front-end's primary function is to optimize half IF rejection, image rejection, and selectivity while providing the first conversion. The front-end uses a varactor-tuned filter that is tuned by the controller. The tuning signal is a DC control voltage between 0 and 9V that come from the PA power control section. Low voltages are for lower frequencies and higher voltages correspond to the higher frequencies. This filter is aligned in the factory and can also be aligned using the Tuner software.

3.4.2.3 Switchable 15 dB Attenuator

This circuit block can provide 0 dB or 15 dB of attenuation in the signal path. Normally, it is set for 0 dB and does not affect the received signal. When strong signals are detected, the radio controller can choose to activate this attenuator to provide protection to the back end circuits, and to enhance high level intermodulation performance. Proprietary algorithms are used to control the switching.

3.4.2.4 Low-Noise Amplifier (LNA, U5302)

A diode (D5281) located after the varactor preselector and before the LNA protects the receiver from strong RF signals by limiting the signal amplitude going into the amplifier. The LNA is a low-noise monolithic IC providing ~ 15 dB of gain to the receiver. It is biased with 5 V and can be bypassed by the radio software under very strong signal conditions.

The UHF receiver also has a second LNA based on Q5252 that can be activated or bypassed by the radio software. This amplifier is protected by D5280 and provides 11 dB of gain. This is available only if the preamplifier option has been purchased.

3.4.2.5 Image Filter

Following the LNA (U5302), the signal goes through a bandpass filter before it is sent to the mixer. The passband is from 380 to 470 MHz with an insertion loss of about 2 dB, while the image rejection is 55 dB. There is a trap on the input side of this filter to attenuate the 109.65 MHz IF.

3.4.2.6 Mixer

A passive double-balanced diode ring mixer is used to down-convert the received signal to an Intermediate Frequency (IF) of 109.65 MHz. The mixer is designed to provide low conversion loss (< 7.0 dBm) and high intermodulation performance and requires a strong injection signal. The mixer is driven by the receiver injection buffer, a two-stage LDMOS IC design, that amplifies the +3 dBm high-side injection signal from the Frequency Generation Unit (FGU) to +24 dBm.

3.4.3 UHF Range 2 (450–520 MHz) Band

The receiver circuits primary duties are to detect, filter, amplify, and demodulate RF signals in the presence of strong interfering noise and unintended signals. The receiver (see Figure 3-15) is broken down into the following blocks:

- Front-end, which includes:
  - High pass fIlter and first low-noise amplifier (LNA)
  - Preselector filter
  - Switchable 15 dB attenuator
  - Second LNA
  - Image Filter
  - First mixer
- Back-end, which includes:
  - Intermediate Frequency (IF)
  - ABACUS III IC

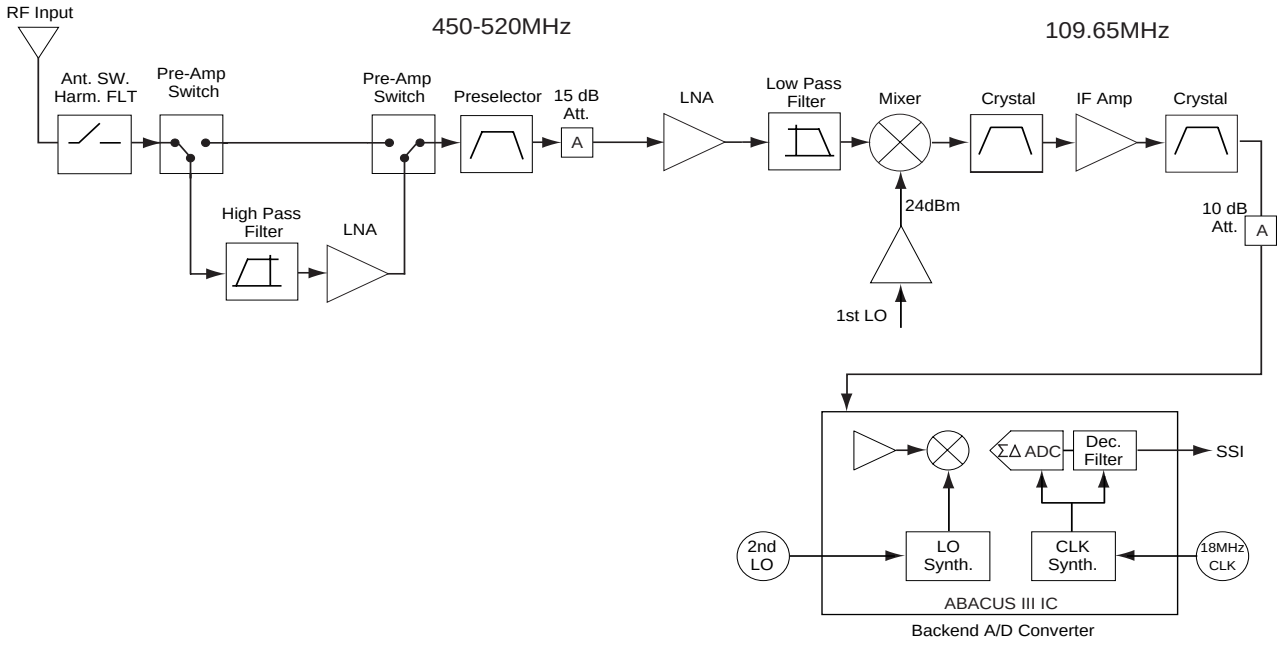

Figure 3-15. Receiver Front-End and Back-End (UHF Range 2)

3.4.3.1 Highpass Filter and First Low-Noise Amplifier

The highpass filter and first low-noise amplifier (LNA) (11 dB gain) can be switched in and out of the signal path by diode switches. When switched into the signal path, the sensitivity of the radio is improved at the cost of degraded intermodulation performance. This can be necessary in fringe areas when strong interference that can lead to intermodulation problems are not present and the desired signal is weak.

The preamplifier version of the radio must be purchased to be able to control this option. If it has not been purchased, the direct path created by the diode switches is the only one available, giving the radio standard model performance with enhanced intermodulation rejection. Purchasing the preamplifier option allows the user to select either mode with the CPS.

3.4.3.2 Preselector Filter

The front-end operates in the 450 to 520 MHz band. The front-end's primary function is to optimize half IF rejection, image rejection, and selectivity while providing the first conversion. The front-end uses a varactor-tuned filter that is tuned by the controller. The tuning signal is a DC control voltage between 0 and 9V that come from the PA power control section. Low voltages are for lower frequencies and higher voltages correspond to the higher frequencies. This filter is aligned in the factory and can also be aligned using the Tuner software.

3.4.3.3 Switchable 15 dB Attenuator

This circuit block can provide 0 dB or 15 dB of attenuation in the signal path. Normally, it is set for 0 dB and does not affect the received signal. When strong signals are detected, the radio controller can choose to activate this attenuator to provide protection to the back end circuits, and to enhance high level intermodulation performance. Proprietary algorithms are used to control the switching.

3.4.3.4 Low-Noise Amplifier (LNA, U5302)

A diode (D5281) located after the varactor preselector and before the LNA protects the receiver from strong RF signals by limiting the signal amplitude going into the amplifier. The LNA is a low-noise monolithic IC providing ~ 15 dB of gain to the receiver. It is biased with 5 V.

The UHF receiver also has a second LNA based on Q5252 that can be activated or bypassed by the radio software. This amplifier is protected by D5280 and provides 11 dB of gain.

3.4.3.5 Image Filter

Following the LNA (U5302), the signal goes through a bandpass filter before it is sent to the mixer. The passband is from 450 to 520 MHz with an insertion loss of about 2 dB, while the image rejection is 55 dB. There is a trap on the input side of this filter to attenuate the 109.65 MHz IF.

3.4.3.6 Mixer

A passive double-balanced diode ring mixer is used to down-convert the received signal to an Intermediate Frequency (IF) of 109.65 MHz. The mixer is designed to provide low conversion loss (< 7.0 dBm) and high intermodulation performance and requires a strong injection signal. The mixer is driven by the receiver injection buffer, a two-stage LDMOS IC design, that amplifies the +3 dBm high-side injection signal from the Frequency Generation Unit (FGU) to +24 dBm.

3.4.4 700–800 MHz Band

The receiver circuits primary duties are to detect, filter, amplify, and demodulate RF signals in the presence of strong interfering noise and unintended signals. The receiver (see Figure 3-16) is broken down into the following blocks:

- Front-end, which includes:
  - Preselector filters
  - Low-noise amplifier (LNA)
  - First mixer
- IF
- Back-end

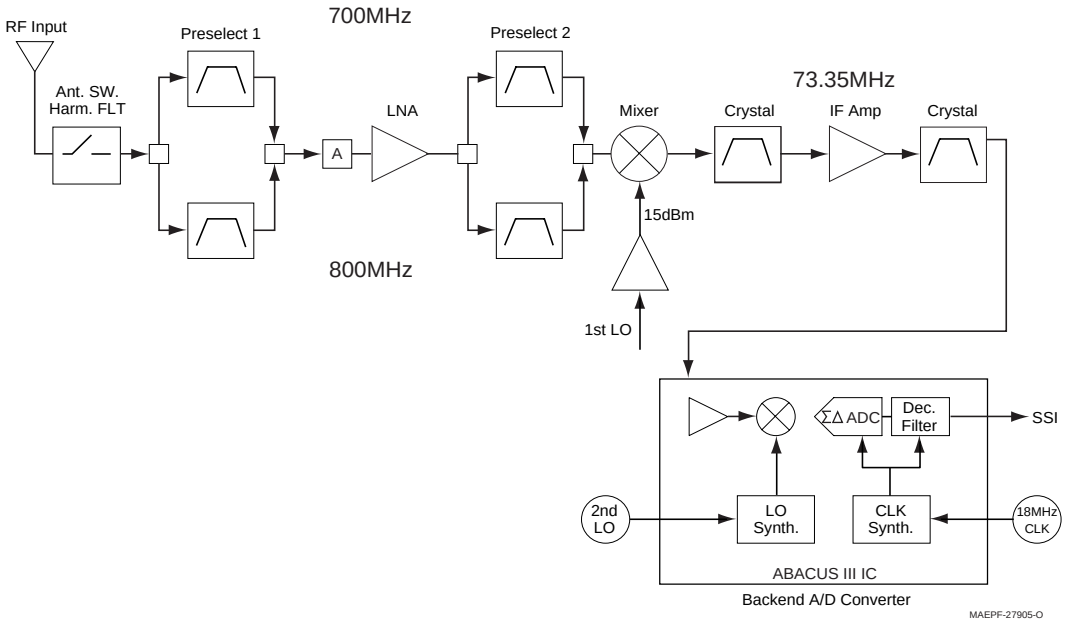

Figure 3-16. Receiver Front-End and Back-End (700–800 MHz)

3.4.4.1 Preselector Filters

The front-end operates in the 700 MHz and 800 MHz bands. The front-end's primary function is to optimize image rejection and selectivity while providing the first conversion. The front- end uses fixed ceramic-filter technology. There are two sets of filters: (B6250 and B6252) for the 800 MHz band and (B6251 and B6253) for the 700 MHz band. These filters are switched between bands by a network of diode switches (D6251 thru D6257) biased by RLC networks (C6254, C6260, R6254, and L6254) that also act as RF chokes. The first filter is a dual-switched filter that reduces the image-frequency response and limits some of the out-of-band interferers. The second filter following the monolithic low-noise amplifier (LNA) provides additional image rejection.

3.4.4.2 Low-Noise Amplifier (LNA, U6250)

A diode (D6258) located after the first preselector and before the LNA protects the receiver from strong RF signals by limiting the signal amplitude going into the amplifier. The LNA is a low-noise monolithic IC providing ~ 16 dB of gain to the receiver. It is biased with 5 V at pins 1 and 6. The input matching consists of an LC network (C6288, L6258) for optimal gain.

3.4.4.3 Mixer (U6251)

The monolithic, passive mixer IC down-converts the received signal to an Intermediate Frequency (IF) of 73.35 MHz. The mixer is designed to provide low conversion loss (< 7.0) and high intermodulation performance. To improve the performance of the mixer in both bands, a shunt 9.1 pF capacitor (C6297) along with a resistive PI network (R6278, R6280, R6281) is designed at the IF port (pin 5) of the mixer. The mixer is driven by the receiver injection buffer, a two-stage discrete/IC design used with the VCO to efficiently drive the mixer over temperature with minimum power variation. The injection buffer provides 15 dBm to the mixer. The VCO does high-side injection for the 800 MHz band and low-side Injection for the 700 MHz band.

3.5 Receiver Back-End

This section discusses the receiver back-end (RXBE) components and detailed theory of operation. The receiver back-end processes the down-converted, filtered IF signal to produce digital data for final processing by the Patriot microcontroller IC.

3.5.1 VHF (136-174 MHz) Band

The receiver back-end contains the following major components:

- Intermediate frequency (IF) section.
- ABACUS III IC

3.5.1.1 Intermediate Frequency (IF) Section

The XTL 5000 radio uses two leadless, surface-mount, two-pole, third-overtone, quartz crystal filters (Y3400, Y3401) separated by a 21 dB gain IF amplifier. The filters are centered at 109.65 MHz. This narrowband bandpass filter contributes to the radio's adjacent-channel and alternate-channel rejection performance. Components L3401, L3403, L3404, L3405, C3421, C3414, C3409, C3416, C3420, C3418 and C3415 are used as impedance-matching networks. Components Q3400, R3409, R3401, R3402, R3405, R3407, and R3413 are used for biasing and stabilizing the transistor Q3400. Components C3424, C3404 bypass the DC supply. L3400 is RF choke. Diode D3400 and Inductor L3408 protect the Abacus and the second IF filter from strong In-band signals.

3.5.1.2 ABACUS III IC

The receiver back-end is designed around the ABACUS III (AD9874 IF digitizing subsystem) IC and its associated circuitry. The AD9874 (Figure 3-17 on page 3-21) is a general-purpose, IF subsystem that digitizes a low-level, 10–300 MHz IF input with a bandwidth up to 270 kHz. The signal chain of the AD9874 consists of a variable gain, low-noise amplifier, a mixer; a bandpass, sigma-delta, A/D converter; and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9874 with 12 dB of continuous gain adjustment. The high dynamic range and inherent anti-aliasing provided by the bandpass, sigma-delta converter allow the AD9874 to cope with blocking signals 80 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers, as well as an SPI port. Input signal RXIF is the 109.65 MHz IF from the IF section in the receiver front-end.

Components C3000, C3038, and L3002 match the input impedance from 50 ohms (IF Filter terminating impedance) to the ABACUS III IC input IFIN. Formatted SSI data is output to the Patriot microcontroller IC for DSP processing on ports FS, DOUTA, and CLKOUT. Control logic is sent to the ABACUS III IC from the Patriot microcontroller via the SPI lines (PC, PD, PE).

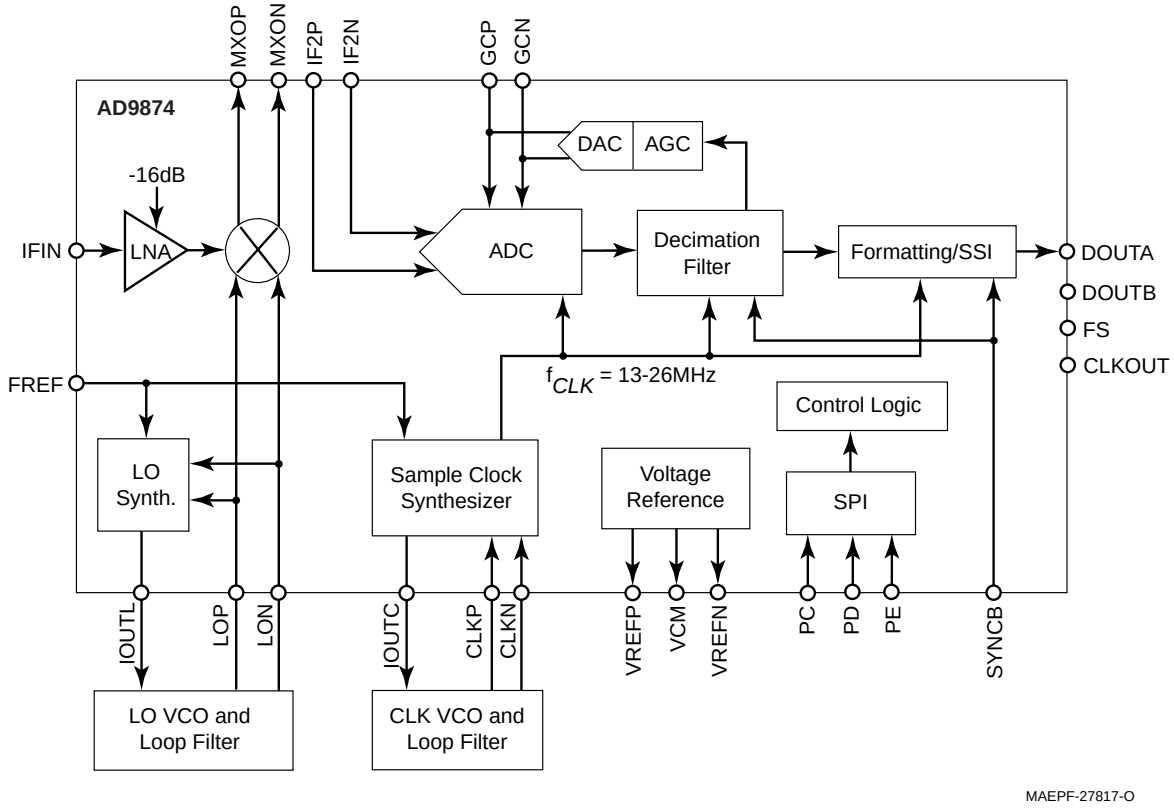

Figure 3-17. ABACUS III (AD9874) IC Functional Block Diagram from Data Sheet (VHF)

3.5.1.2.1 Second Local Oscillator

The ABACUS III IC local oscillator (LO) synthesizer controls the second LO. Signal FREF is the 16.8 MHz reference from the frequency generation unit (FGU). The second LO frequency is 107.4 MHz by default, or 111.9 MHz in special cases as necessary to avoid radio self-quieters. The second LO signal mixes with IFIN to produce a 109.65 MHz final IF. The external VCO consists of transistor Q3000, together with its bias and instability network and tank elements. Darlington transistor Q3001 along with C3035 and C3017 form an active DC filter. The second-order loop filter is comprised of C3044, C3005, and R3009.

3.5.1.2.2 Sampling Clock Oscillator

The ABACUS III IC sampling clock synthesizer, at Fclk=18 MHz (IF2=Fclk/8, where Fclk is the clock rate), utilizes a negative-resistance core that is internal to the ABACUS III IC which, when used in conjunction with an external LC tank (made up of L3003 and C3039) and a varactor (D3001), serves as the VCO.

3.5.2 UHF Range 1 (380-470 MHz) Band

The receiver back-end (see Figure 3-14 on page 3-15) contains the following major components:

- Intermediate frequency (IF) filter
- ABACUS III IC

3.5.2.1 Intermediate Frequency (IF) Filter

The XTL 5000 radio uses two leadless, surface-mount, two-pole, third-overtone, quartz crystal filters (Y5400, Y5401) separated by a 20 dB gain IF amplifier. The filter is centered at 109.65 MHz. This narrow-bandpass filter gives the radio part of its adjacent-channel and alternate-channel rejection performance. Impedance-matching networks are located at the input and output of each crystal. The IF amplifier is made with Q5401. The 10 dB attenuator (U5400) located after the second crystal filter is controlled by the software to limit the signal gain in front of the ABACUS III IC.

3.5.2.2 ABACUS III IC (U5002)

The receiver back-end is designed around the ABACUS III (AD9874 IF digitizing subsystem) IC and its associated circuitry. The AD9874 (Figure 3-18) is a general-purpose, IF subsystem that digitizes a low-level, 10-300 MHz IF input with a bandwidth up to 270 kHz. The signal chain of the AD9874 consists of a variable gain, low-noise amplifier, a mixer; a bandpass, sigma-delta, A/D converter; and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9874 with 12 dB of continuous gain adjustment. The high dynamic range and inherent anti-aliasing provided by the bandpass, sigma-delta converter allow the AD9874 to cope with blocking signals 80 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers, as well as an SPI port. Input signal RXIF is the 109.65 MHz IF from the IF filter.

Components C5002, C5007, and L5002 match the input impedance from 50 ohms (IF Filter terminating impedance) to the ABACUS III IC input IFIN. Formatted SSI (synchronous serial interface) data is output to the Patriot microcontroller IC for DSP processing on ports FS, DOUTA, and CLKOUT. Control logic is sent to the ABACUS III IC from the Patriot microcontroller via the SPI lines (PC, PD, PE).

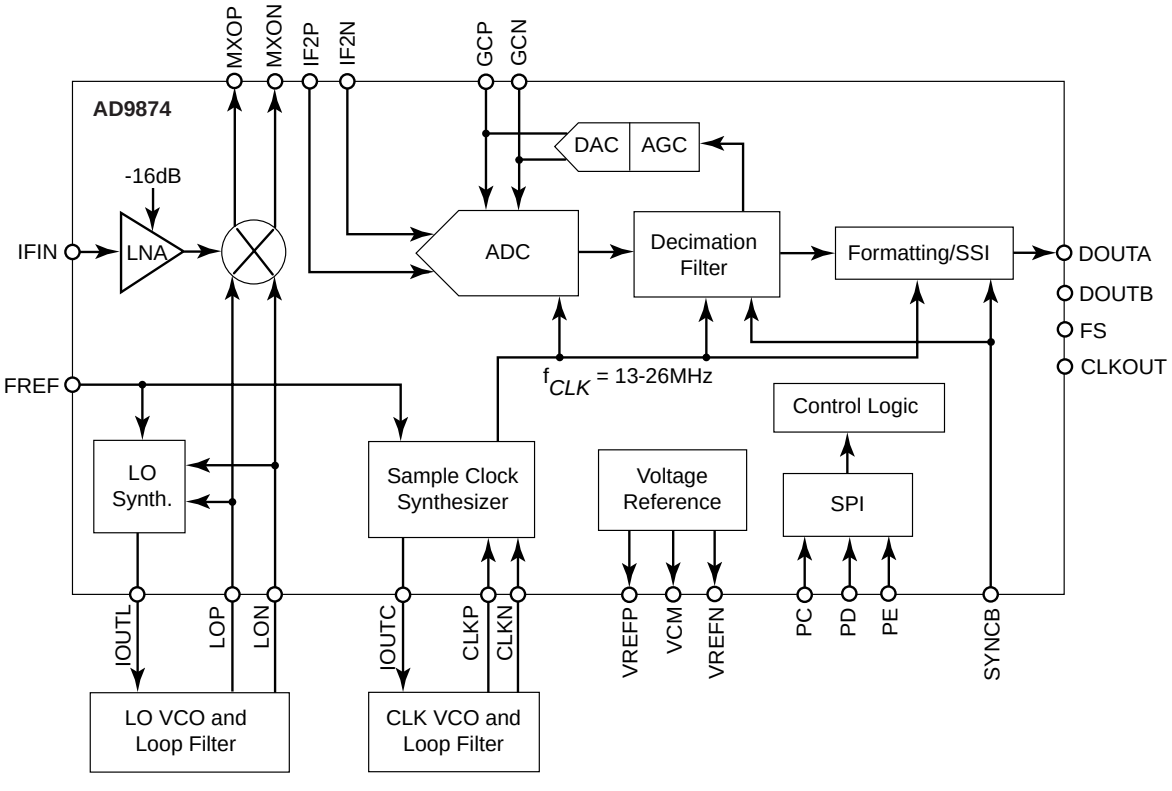

Figure 3-18. ABACUS III (AD9874) IC Functional Block Diagram from Data Sheet (UHF Range 1)

3.5.2.2.1 Second Local Oscillator (LO)

The ABACUS III IC local oscillator (LO) synthesizer controls the second LO. Signal FREF is the 16.8 MHz reference from the frequency generation unit (FGU). The second LO frequency is 107.4 MHz by default, or 111.9 MHz in special cases as necessary to avoid radio self-quieters. The second LO signal mixes with IFIN to produce a 2.25 MHz final IF. The external VCO consists of transistor Q5002, together with its bias and instability network and tank elements. Darlington transistor Q5001 along with C5018 and C5050 form an active DC filter. The 2nd order loop filter is comprised of C5044, C5045, and R5013.

3.5.2.2.2 Sampling Clock Oscillator

The ABACUS III IC sampling clock synthesizer, at Fclk=18 MHz (IF2=Fclk/8, where Fclk is the clock rate), utilizes the clock VCO built around Q5003.

3.5.3 UHF Range 2 (450-520 MHz) Band

The receiver back-end (see Figure 3-15 on page 3-17) contains the following major components:

- Intermediate frequency (IF) filter
- ABACUS III IC

3.5.3.1 Intermediate Frequency (IF) Filter

The XTL 5000 radio uses two leadless, surface-mount, two-pole, third-overtone, quartz crystal filters (Y5400, Y5401) separated by a 20 dB gain IF amplifier. The filter is centered at 109.65 MHz. This narrow-bandpass filter gives the radio part of its adjacent-channel and alternate-channel rejection performance. Impedance-matching networks are located at the input and output of each crystal. The IF amplifier is made with Q5401. The 10 dB attenuator (U5400) located after the second crystal filter is controlled by the software to limit the signal gain in front of the ABACUS III IC.

3.5.3.2 ABACUS III IC (U5002)

The receiver back-end is designed around the ABACUS III (AD9874 IF digitizing subsystem) IC and its associated circuitry. The AD9874 (Figure 3-19 on page 3-24) is a general-purpose, IF subsystem that digitizes a low-level, 10-300 MHz IF input with a bandwidth up to 270 kHz. The signal chain of the AD9874 consists of a variable gain, low-noise amplifier, a mixer; a bandpass, sigma-delta, A/D converter; and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9874 with 12 dB of continuous gain adjustment. The high dynamic range and inherent anti-aliasing provided by the bandpass, sigma-delta converter allow the AD9874 to cope with blocking signals 80 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers, as well as an SPI port. Input signal RXIF is the 109.65 MHz IF from the IF filter.

Components C5002, C5007, and L5002 match the input impedance from 50 ohms (IF Filter terminating impedance) to the ABACUS III IC input IFIN. Formatted SSI (synchronous serial interface) data is output to the Patriot microcontroller IC for DSP processing on ports FS, DOUTA, and CLKOUT. Control logic is sent to the ABACUS III IC from the Patriot microcontroller via the SPI lines (PC, PD, PE).

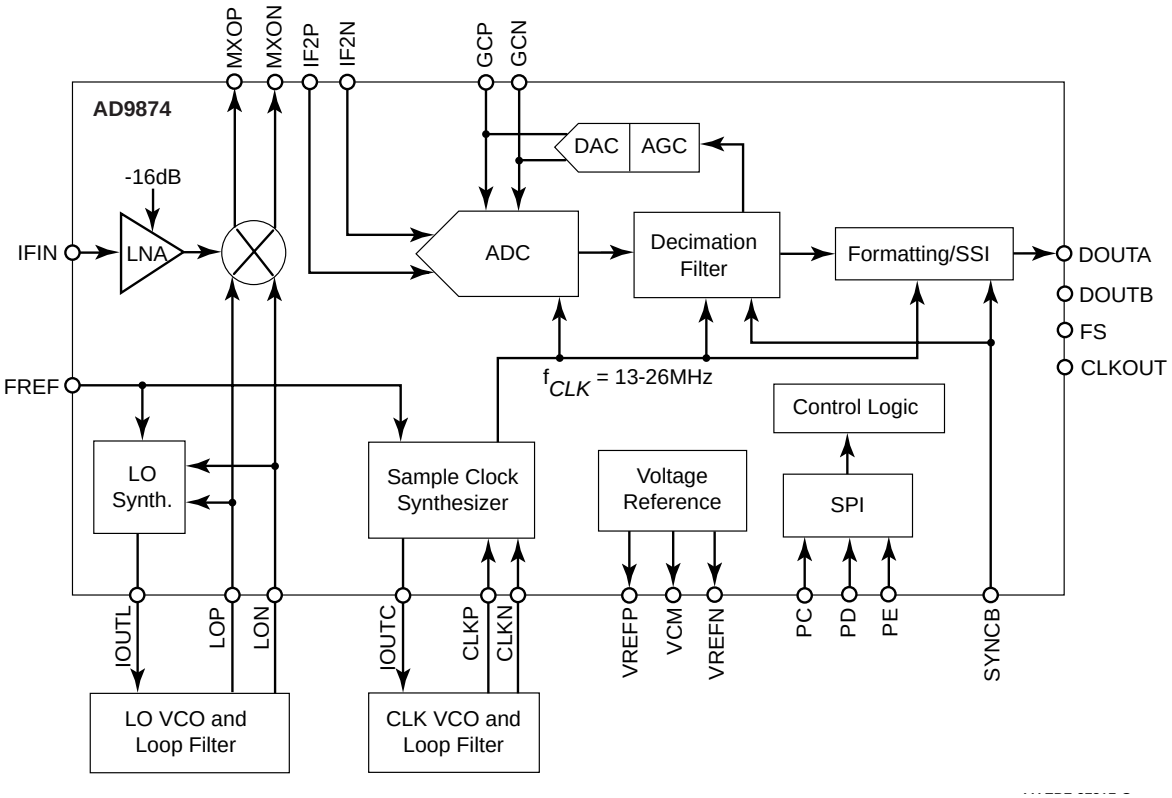

Figure 3-19. ABACUS III (AD9874) IC Functional Block Diagram from Data Sheet (UHF Range 2)

3.5.3.2.1 Second Local Oscillator (LO)

The ABACUS III IC local oscillator (LO) synthesizer controls the second LO. Signal FREF is the 16.8 MHz reference from the frequency generation unit (FGU). The second LO frequency is 107.4 MHz by default, or 111.9 MHz in special cases as necessary to avoid radio self-quieters. The second LO signal mixes with IFIN to produce a 2.25 MHz final IF. The external VCO consists of transistor Q5002, together with its bias and instability network and tank elements. Darlington transistor Q5001 along with C5018 and C5050 form an active DC filter. The 2nd order loop filter is comprised of C5044, C5045, and R5013.

3.5.3.2.2 Sampling Clock Oscillator

The ABACUS III IC sampling clock synthesizer, at Fclk=18 MHz (IF2=Fclk/8, where Fclk is the clock rate), utilizes the clock VCO built around Q5003.

3.5.4 700–800 MHz Band

The receiver back-end (see Figure 3-16 on page 3-19) contains the following major components:

- Intermediate frequency (IF) filter
- ABACUS III IC

3.5.4.1 Intermediate Frequency (IF) Filter

The XTL 5000 radio uses two leadless, surface-mount, two-pole, third-overtone, quartz crystal filters (B6350, B6351) separated by a 20 dB gain IF amplifier. The filter is centered at 73.35 MHz. This narrow-bandpass filter gives the radio its adjacent-channel and alternate-channel rejection performance. Components L6350, L6351, L6352, L6353, C6351, C6352, C6353, C6355, C6356, and C6357 are used as impedance-matching networks. Components L6355, R6354, R6352, R6353, C6354, and R6350 are used for biasing and stabilizing the transistor Q6350. Component C6358 bypasses the DC supply. L6355 is an RF choke.

3.5.4.2 ABACUS III IC (U6000)

The receiver back-end is designed around the ABACUS III (AD9874 IF digitizing subsystem) IC and its associated circuitry. The AD9874 (Figure 3-20) is a general-purpose, IF subsystem that digitizes a low-level, 10–300 MHz IF input with a bandwidth up to 270 kHz. The signal chain of the AD9874 consists of a variable gain, low-noise amplifier, a mixer; a bandpass, sigma-delta, A/D converter; and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9874 with 12 dB of continuous gain adjustment. The high dynamic range and inherent anti-aliasing provided by the bandpass, sigma-delta converter allow the AD9874 to cope with blocking signals 80 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers, as well as an SPI port. Input signal RXIF is the 73.35 MHz IF from the IF filter in the receiver front-end.

Components C6000, C6001, and L6000 match the input impedance from 50 ohms (IF Filter terminating impedance) to the ABACUS III IC input IFIN. Formatted SSI (synchronous serial interface) data is output to the Patriot microcontroller IC for DSP processing on ports FS, DOUTA, and CLKOUT. Control logic is sent to the ABACUS III IC from the Patriot microcontroller via the SPI lines (PC, PD, PE).

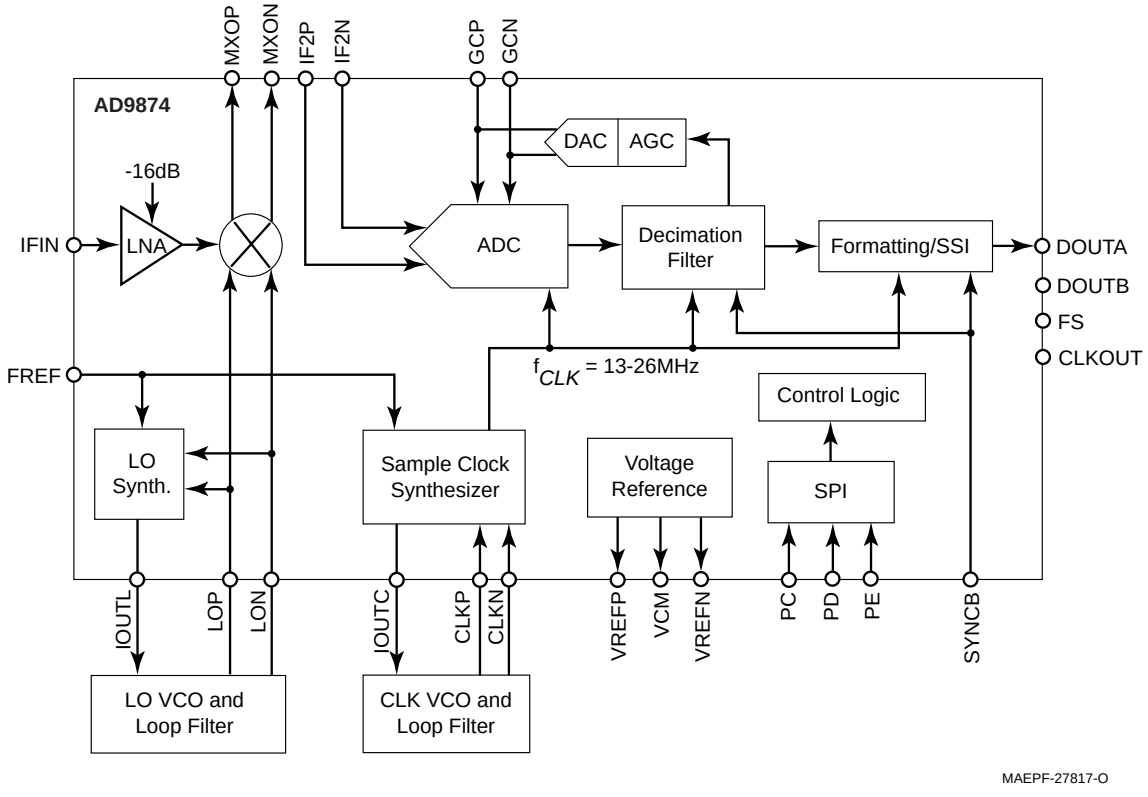

Figure 3-20. ABACUS III (AD9874) IC Functional Block Diagram from Data Sheet (700–800 MHz)

3.5.4.2.1 Second Local Oscillator (LO)

The ABACUS III IC local oscillator (LO) synthesizer controls the second LO. Signal FREF is the 16.8 MHz reference from the frequency generation unit (FGU). The second LO frequency is 75.6 MHz by default, or 71.1 MHz in special cases as necessary to avoid radio self-quieters. The second LO signal mixes with IFIN to produce a 2.25 MHz final IF. The external VCO consists of transistor Q6000, together with its bias and instability network and tank elements. Darlington transistor Q6001 along with C6024 and C6025 form an active DC filter. The 2nd order loop filter is comprised of C6056, C6057, and R6019.

3.5.4.2.2 Sampling Clock Oscillator

The ABACUS III IC sampling clock synthesizer, at Fclk=18 MHz (IF2=Fclk/8, where Fclk is the clock rate), utilizes a negative-resistance core that is internal to the ABACUS III IC which, when used in conjunction with an external LC tank (made up of L6003 and C6031) and a varactor (D6030), serves as the VCO.

3.6 Transmitter

This section of the theory of operation provides a detailed circuit description of the transmitter, which includes the RF power amplifier (RFPA), output network (ON), and power control.

When reading the theory of operation, refer to the appropriate schematic and component location diagrams located in “Chapter 7. Schematics, Component Location Diagrams, and Parts Lists”. This detailed theory of operation will help isolate the problem to a particular component. However, first use the *ASTRO Digital XTL 5000 VHF/UHF Range 1/UHF Range 2/700–800 MHz Mobile Radio Basic Service Manual* to troubleshoot the problem to a particular section.

3.6.1 VHF (136-174 MHz) Band

3.6.1.1 50-Watt Transmitter

The following text discusses the 50-W transmitter.

3.6.1.1.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-21.

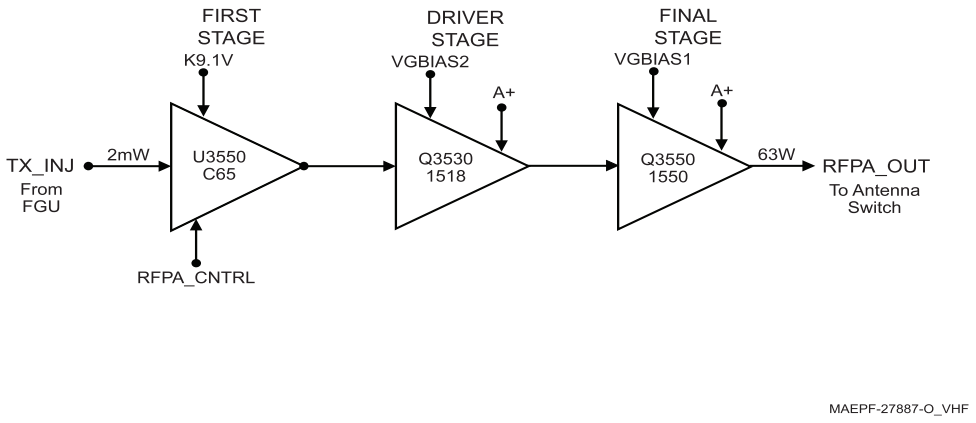

Figure 3-21. 50-Watt RF Power Amplifier (RFPA) Gain Stages (VHF)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See “3.6.1.4. Power Control (for 50W and 100W Transmitter)” on page 3-30 for a detailed explanation of the power control section.

The 2 mW TX_INJ signal is routed to the U3550 first-stage device (Pin 16, RFIN) via C3500 to an integrated, wide-band input match. U3550 is a two-stage LDMOS device with a bandpass interstage match consisting of C3503, L3502, C3504, R3501 and C3505 routed between VD1 (pin 14) and G2 (pin 11). L3501 and L3503 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U3550 stages are operated Class A.

Driver Stage

C3521, L3520, C3520, and a transmission line form a low-pass, interstage match that transfers power to the Q3530 LDMOS transistor. R3520-3 provide device stability, and R3524 and C3522 supply the VGBIAS2 gate bias. L3530-1, R3530-1, C3530, C3531, C3536 and C3537 form the A+ drain bias circuit. Q3530 is operated Class AB.

Final Stage

C3532-4, and transmission lines form a bandpass. R3532-8 provide stability for Q3550. R3540 and C3535 supply the VGBIAS1 gate bias to Q3550. L3549-51, C3548-51, and R3551 form the A+ drain bias circuit.

C3552-9 and transmission lines form a low-pass. Q3550 operate Class AB.

R3550, R3560, C3563, and U3561 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R3560 sets the circuit gain. U3560 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.1.2 100-Watt Transmitter

The following text discusses the 100-W transmitter.

3.6.1.2.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-22.

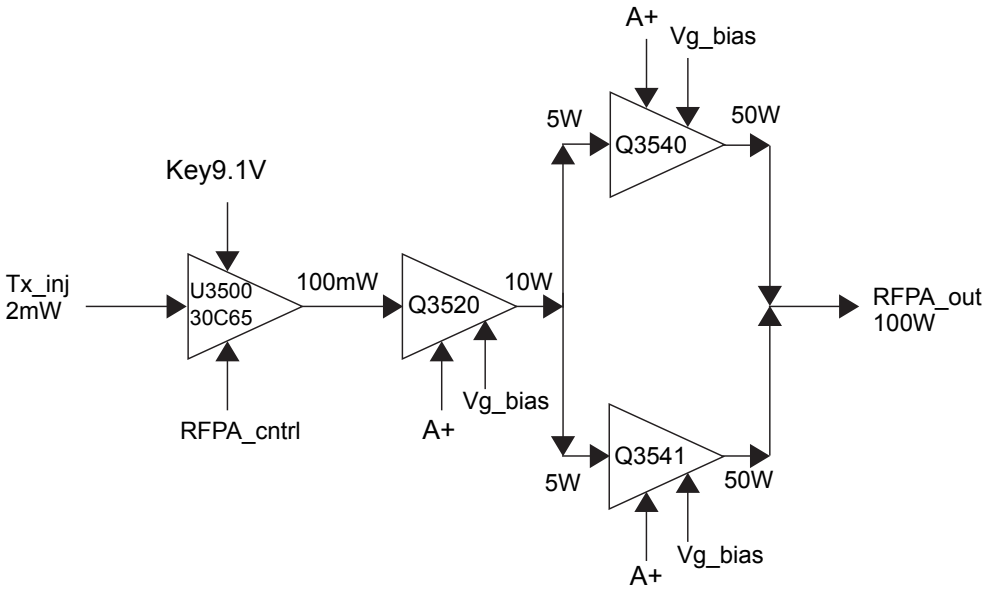

Figure 3-22. 100-Watt RF Power Amplifier (RFPA) Gain Stages (VHF)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See "3.6.1.4. Power Control (for 50W and 100W Transmitter)" on page 3-30 for a detailed explanation of the power control section.

The 2 mW TX_INJ signal is routed to the U3500 first-stage device (Pin 16, RFIN) via C3500 to an integrated, wide-band input match. U3550 is a two-stage LDMOS device with a bandpass interstage match consisting of C3502 and L3501 routed between VD1 (pin 14) and G2 (pin 11). L3501 and L3500 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U3500 stages are operated Class A.

Driver Stage

C3521, L3520, C3520, and a transmission line form a low-pass, interstage match that transfers power to the Q3520 LDMOS transistor. R3520-5 provide device stability, and R3526 and C3522 supply the VGBIAS2 gate bias. L3521, R3528, C3525, C3524, C3536, L3522 and R3527 form the A+ drain bias circuit. Q3520 is operated Class AB.

Dual Final Stage

C3540-1, C3543-4 and transmission lines form a bandpass. R3541-8 provide stability for Q3540. R3550-7 provide stability for Q3541. R3540 and R3568 supply the VGBIAS1 gate bias to Q3540. R3569 and R3558 supply the VGBIAS2 gate bias to Q3541. L3540-4 and C3560-1 form the A+ drain bias circuit. C3548-55 and transmission lines form a low-pass. Q3540-1 operate Class AB.

R3560-1, C3561, and U3561 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R3564 sets the circuit gain. U3560 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.1.3 Output Network (ON) - (for 50W and 100W Transmitter)

The ON consists of the antenna switch, harmonic filter, and power detector (see Figure 3-23).

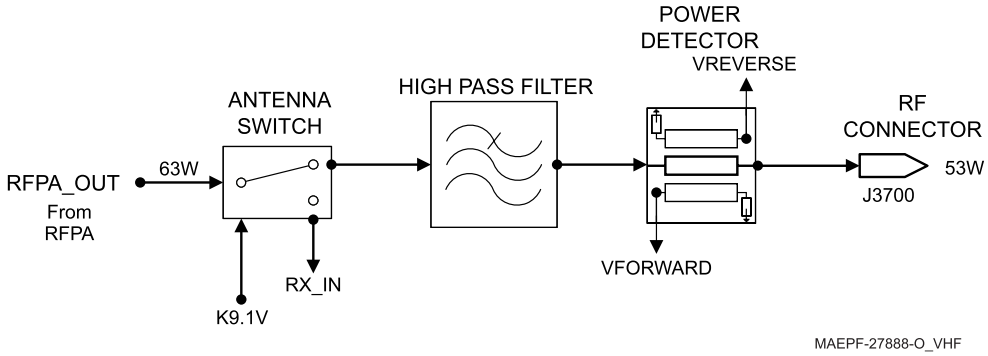

Figure 3-23. Output Network Components (VHF)

Antenna Switch

The antenna switch functions in two modes, which are determined by the presence of K9.1V. The K9.1V switch bias is applied via L3700, L3731-2, and C3702. When K9.1V is present, the switch is in TX mode. D3701-2 and D3704 are forward biased forming a low-loss path from the RFPA final stage to the harmonic filter and a 60 dB isolation path between the RFPA final stage and the RX front-end. Isolation is achieved via a quarter-wave transmission line between D3701 and D3702. D3701-4 serves as an ESD protection circuit against ESD discharge on the antenna connector.

When K9.1V is absent, the switch is in RX mode. D3701 and D3702 are reverse biased forming a low-loss path from the harmonic filter to the RX front-end and a 60 dB isolation path from the harmonic filter to the RFPA final stage. Isolation is achieved via the D3701 off resistance.

Harmonic Filter

L3720-7, C3720-3, form the twelve-element, low-pass harmonic filter. The filter attenuates harmonics generated by the RFPA when the antenna switch is in TX mode and provides extra selectivity when the antenna switch is in RX mode.

Power Detector

The power detector consists of two asymmetric, coupled transmission lines and detection circuitry that detects forward and reverse power. C3730-1, D3730, L3730, R3730-3, and R3735-6 form the forward-power detector (VFORWARD), which is used for power leveling. C3732-3, D3731, L3731, R3737-9, and R3733-4 form the reverse-power detector (VREVERSE). L3737 provides an electrostatic discharge path to protect the RFPA final stage device.

3.6.1.4 Power Control (for 50W and 100W Transmitter)

The power control section is comprised of a control loop to level forward power and protection mechanisms to reduce power to a safe level for the given environmental conditions (see Figure 3-24).

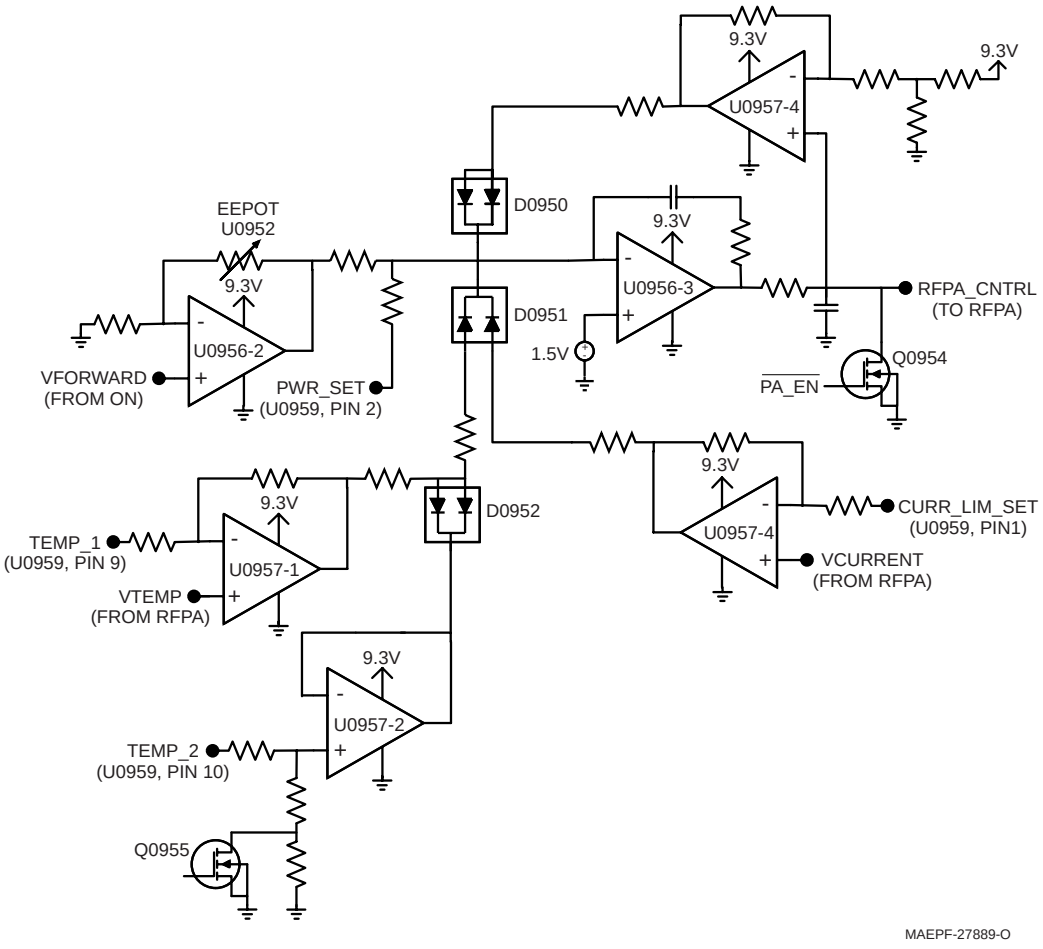

Figure 3-24. Power Control Components (VHF)

Power Control Loop

VFORWARD from the ON is buffered via the non-inverting, variable-gain stage U0956-2 whose gain is set by EPOT U0952. The proper gain is determined during power-detection calibration tuning. Buffered VFORWARD (U0956-2, Pin 7) is added to PWR_SET via R0971, R0972, and R0947 and then compared to a reference determined by R0974 and R0975. PWR_SET is supplied by the digital-to-analog converter (DAC) U0959, Pin 2. Comparator stage U0956-3 increases or decreases RFPA_CNTRL so that the voltage at U0956-3, Pin 9 in the same at the reference voltage at U0956-3, Pin 10. When the PWR_SET voltage is decreased, U0956-3 increases RFPA_CNTRL to increase VFORWARD which is proportional to forward power thus increasing the power level. When the PWR_SET voltage is increased, U0956-3 decreases RFPA_CNTRL to decrease VFORWARD, thus decreasing the power level. The microprocessor initiates the loop through U0958-1 and Q0954. Loop timing is set via software together with R0977, and C0973.

Protection Mechanisms

Final-stage temperature is sensed in the RFPA resulting in VTEMP, which is proportional to temperature. VTEMP is compared against a reference voltage TEMP_1 (U0959, pin 9) via U0957-1. When VTEMP exceeds TEMP_1, the U0957-1, pin 1, voltage increases and forward biases one of the D0951 diodes, which cuts back power. Power continues to cut back with rising temperature until the voltage level at the junction of R0978 and R0983 is high enough to forward bias D0952, thus clamping the cut back so that the radio meets its duty cycle specification while providing protection against high-temperature conditions. The clamping level is set via TEMP_2 (U0959, pin 10) and U0957-2. U0957-3 is used to sense if a high A+ battery voltage condition exists and, if it does, the Q0955 gate is biased on, which increases the clamp voltage allowing for additional power cutback for a high A+, high temperature condition.

Final-stage current is also monitored via VCURRENT, which is proportional to current. VCURRENT is compared against a reference CURR_LIM_SET (U0959, pin 1) which is tuned after power characterization. If VCURRENT exceeds CURR_LIM_SET, then U0957-4, pin 14, voltage rises and forward biases one of the D0951 diodes, which limits power.

Finally, control voltage is limited by U0956-4 and D0950. RFPA_CNTRL can rise to the control voltage limit set by R0942-4.

3.6.2 UHF Range 1 (380-470 MHz) Band

3.6.2.1 40-Watt Transmitter

The following text discusses the 40-W transmitter.

3.6.2.1.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-25.

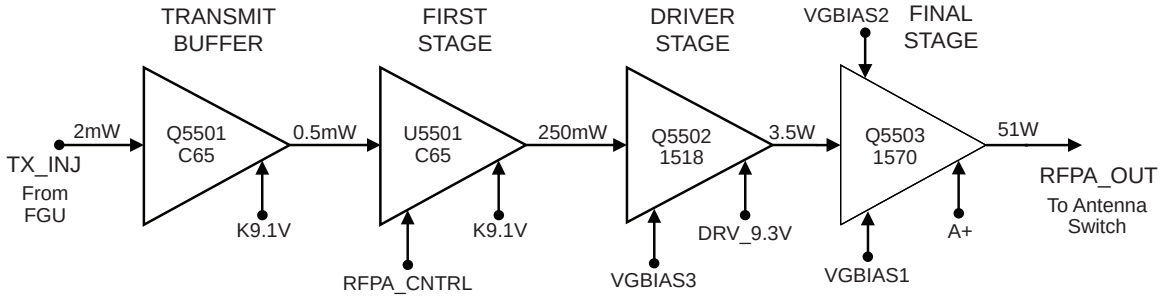

Figure 3-25. 40-Watt RF Power Amplifier (RFPA) Gain Stages (UHF Range 1)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See “3.6.2.4. Power Control (for 40W and 100W Transmitter)” on page 3-35 for a detailed explanation of the power control section.

The 0.5 mW TX_INJ signal is routed to the U5501 first stage device (Pin 16, RFIN) via C5508 to an integrated, wide-band input match. U5501 is a two-stage LDMOS device with a bandpass interstage match consisting of L5503, C5507, and C5509 routed between VD1 (pin 14) and G2 (pin 11). L5502 and L5505 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U5501 stages are operated Class A and the second-stage output power is approximately 250 mW.

Driver Stage

C5566, C5516, C5518 and a transmission line form a low-pass, interstage match that transfers power to the Q5502 LDMOS transistor. R5511-R5515 provide device stability, and R5527, C5556, C5525 and R5516 supply the VGBIAS3 gate bias. L5508, C5527, R5517, E5501 and C5526 form the 9.3 V drain bias circuit. The 9.3 V drain voltage is supplied from regulator U5570 via R5574. The 9.3 V supply to the driver is only present during transmit and is disabled during receive via the K9.1V signal and Q5570. Q5502 is operated Class AB and its output power is approximately 3.5 W.

Final Stage

C5559, C5560, C5535, C5538, and transmission lines form a low pass, splitter match that transfers power to the LDMOS final-stage transistor Q5503. Q5503 contains two transistors in a single package, each with it's own gate and drain lead. R5530, R5533, R5534 and R5536 provide stability for Q5503. R5525, C5557, C5539 and R5520 supply the VGBIAS1 gate bias to Q5503-7. R5526, C5558, C5540 and R5521 supply the VGBIAS2 gate bias to Q5503-6. L5510, C5549, R5523, E5502 and C5550 form the A+ drain bias circuit to Q5503-2 and Q5503-3. C5542-43, C5545-46, C5547-48, C5551-53 and transmission lines form a low -pass combiner match that transfers approximately 51 W to the antenna switch. R5535 provides stability for Q5503. Q5503 operates Class AB.

R5522 and U5503 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R5519 sets the circuit gain. U5502 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.2.2 100-Watt Transmitter

The following text discusses the 100-W transmitter.

3.6.2.2.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-26.

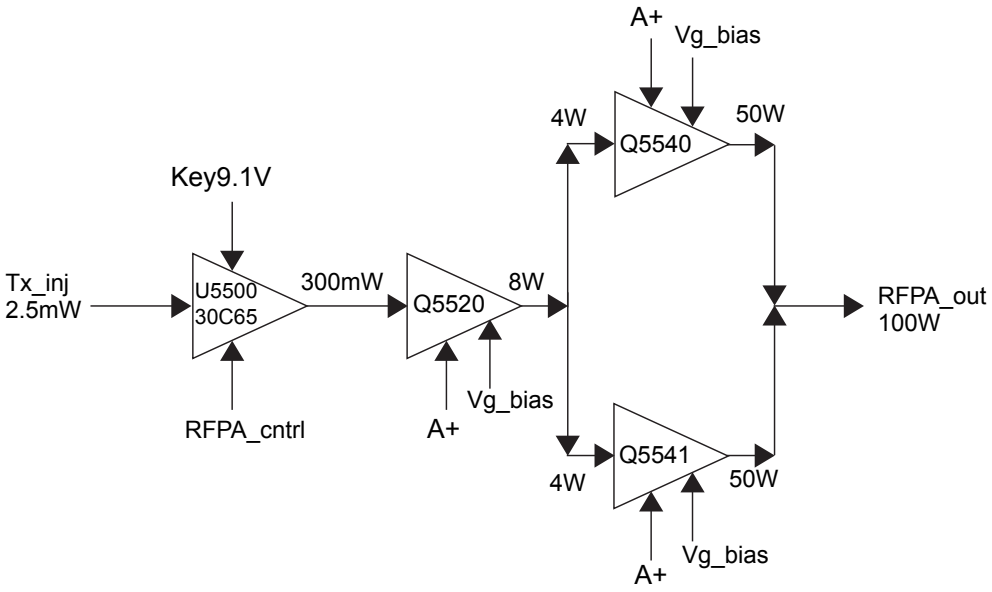

Figure 3-26. 100-Watt RF Power Amplifier (RFPA) Gain Stages (UHF Range 1)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See "3.6.2.4. Power Control (for 40W and 100W Transmitter)" on page 3-35 for a detailed explanation of the power control section.

The 2.5 mW TX_INJ signal is routed to the U5500 first stage device (Pin 16, RFIN) via C5524 to an integrated, wide-band input match. U5500 is a two-stage LDMOS device with a bandpass interstage match consisting of L5511, L5510, C5511 routed between VD1 (pin 14) and G2 (pin 11). L5510 and R5510 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U5501 stages are operated Class A and the second-stage output power is approximately 300 mW.

Driver Stage

C5525, L5514, C5516, C5518, C5519, C5523 and a transmission line form a low-pass, interstage match that transfers power to the Q5502 LDMOS transistor. R5520-R5525 provide device stability, and R5526, C5520 and C5529 supply the VGBIAS3 gate bias. L5520, C5521, R5527, L5521, R5528 and C5522 form the A+ drain bias circuit. Q5520 is operated Class AB and its output power is approximately 8 W.

Dual Final Stage

C5530, C5531, C5532, C5533, C5536, C5537-41 and transmission lines form a low pass, splitter match that transfers power to the LDMOS dual final-stage transistors Q5541 and Q5540. Q5540 and Q5541 contain two transistors in a single package, each with it's own gate and drain lead. R5542-5, R5548-51 provide stability for Q5540. R5552-5, R5557-60 provide stability for Q5541. R5546, C5602 and C5542 supply the VGBIAS1 gate bias to Q5540. R5581, C5550 and C5603 supply the VGBIAS2 gate bias to Q5541. L5543, L5544, R5574, C5567 and C5568 form the A+ drain bias circuit to Q5540 and Q5541. C5551-56, C5559-66, C5584, C5587, C5589 and transmission lines form a low -pass combiner match that transfers approximately 100 W to the antenna switch. R5562 provides stability for Q5540. R5573 provides stability for Q5541. Both Q5540 and Q5541 operate Class AB.

R5575 and U5561 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R5578 sets the circuit gain. U5560 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.2.3 Output Network (ON) - (for 40W and 100W Transmitter)

The ON consists of the antenna switch, harmonic filter, and power detector (see Figure 3-27).

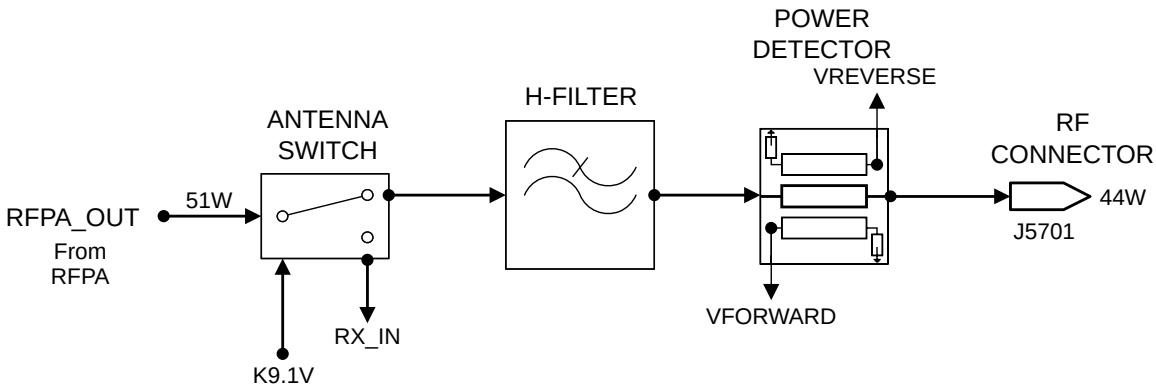

Figure 3-27. Output Network Components (UHF Range 1)

Antenna Switch

The antenna switch functions in two modes determined by the presence of K9.1V. The K9.1V switch bias is applied via L5701and C5702. When K9.1V is present, the switch is in TX mode. D5701, D5702 and D5703 are forward biased forming a low-loss path from the RFPA final stage to the harmonic filter and a 20 dB isolation path between the RFPA final stage and the RX front-end. Isolation is achieved via a quarter-wave transmission lines between D5701 - D5702 and between D5702 - D5703. C5709-10 resonates out the D5702-3 on inductance improving the isolation. When K9.1V is absent, the switch is in RX mode. D5701, D5702 and D5703 are reverse biased forming a low-loss path from the harmonic filter to the RX front-end and a 20 dB isolation path from the harmonic filter to the RFPA final stage. Isolation is achieved via the D5701 off resistance. L5702 resonates out the D5701 off capacitance improving the isolation.

Harmonic Filter

The harmonic filter is a 7-element, equal-L Zolotarev quasi-lowpass filter consisting of C5712 and C5713, C5719 thru C5721 and L5706 thru L5708. L5712, C5711 and L5713, C5714 form two shunt zeros for extra attenuation at the second harmonic. C5708 acts as a DC block between the filter and the antenna switch. The filter provides approximately 60 dB of harmonic rejection. The harmonic filter together with the antenna switch provides approximately 0.7 dB insertion loss between the transmitter power amplifier and the antenna.

Power Detector

The power detector consists of a main microstrip transmission line that transfers power from the harmonic filter to the antenna and two parallel lines that are used to detect the forward and reverse power. The forward power detection line is terminated via R5707 and R5708. RF energy coupled onto this line is rectified and filtered via D5704 and C5715 to provide a DC voltage to the power control circuitry that is proportional to the forward transmitted power level. The detected forward voltage is approximately 1.5 Vdc when the radio is putting out 44 watts. Thermister R5704 compensates for temperature changes in D5704 to maintain constant DC voltage versus detected forward power over temperature.

The reverse power detection line is terminated via R5705-06. RF energy coupled onto this line is rectified and filtered via D5705 and C5718 to provide a DC voltage to the power control circuitry that is proportional to the reverse power level reflected back from the antenna. Thermister R5712 compensates for temperature changes in D5705 to maintain constant DC voltage versus detected reverse power over temperature.

3.6.2.4 Power Control (for 40W and 100W Transmitter)

The power control section is comprised of a control loop to level forward power, and protection mechanisms to reduce power to a safe level for the given environmental conditions (see Figure 3-28 on page 3-36).

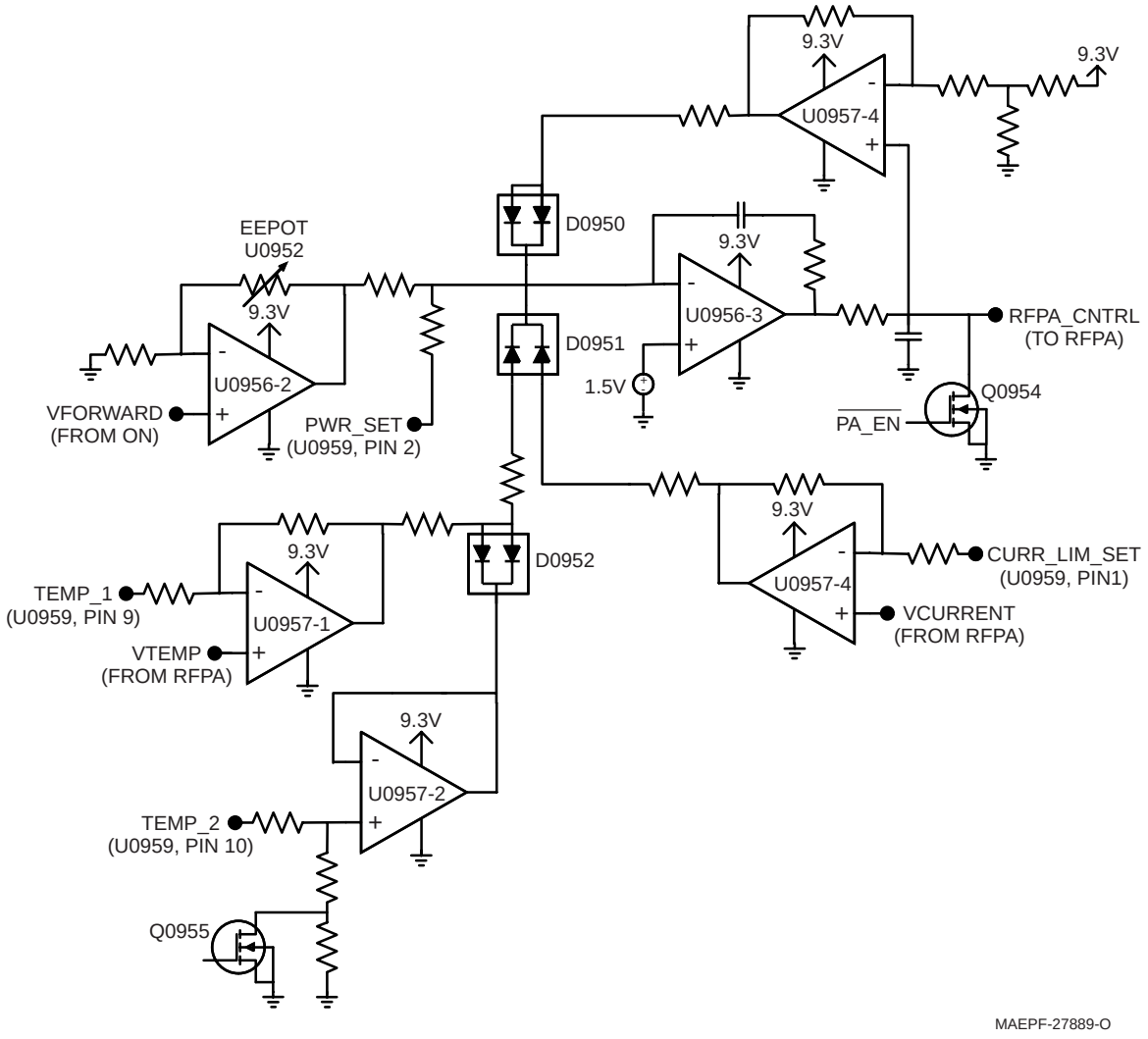

Figure 3-28. Power Control Components (UHF Range 1)

Power Control Loop

VFORWARD from the ON is buffered via the non-inverting, variable-gain stage U0956-2 whose gain is set by EPOT U0952. The proper gain is determined during power-detection calibration tuning. Buffered VFORWARD (U0956-2, Pin 7) is added to PWR_SET via R0971 and R0972 and then compared to a reference determined by R0974 and R0975. PWR_SET is supplied by the digital-to-analog converter (DAC) U0959, Pin 2. Comparator stage U0956-3 increases or decreases RFPA_CNTRL so that the voltage at U0956-3, Pin 9 in the same at the reference voltage at U0956-3, Pin 10. When the PWR_SET voltage is decreased, U0956-3 increases RFPA_CNTRL to increase VFORWARD which is proportional to forward power thus increasing the power level. When the PWR_SET voltage is increased, U0956-3 decreases RFPA_CNTRL to decrease VFORWARD, thus decreasing the power level. The microprocessor initiates the loop through U0958-1 and Q0954. Loop timing is set via software together with R0977 and C0973.

Protection Mechanisms

Final-stage temperature is sensed in the RFPA resulting in VTEMP, which is proportional to temperature. VTEMP is compared against a reference voltage TEMP_1 (U0959, pin 9) via U0957-1. When VTEMP exceeds TEMP_1, the U0957-1, pin 1, voltage increases and forward biases one of the D0951 diodes, which cuts back power. Power continues to cut back with rising temperature until the voltage level at the junction of R0978 and R0983 is high enough to forward bias D0952, thus clamping the cut back so that the radio meets its duty cycle specification while providing protection against high-temperature conditions. The clamping level is set via TEMP_2 (U0959, pin 10) and U0957-2. U0957-3 is used to sense if a high A+ battery voltage condition exists and, if it does, the Q0955 gate is biased on, which increases the clamp voltage allowing for additional power cutback for a high A+, high temperature condition.

Final-stage current is also monitored via VCURRENT, which is proportional to current. VCURRENT is compared against a reference CURR_LIM_SET (U0959, pin 1) which is tuned after power characterization. If VCURRENT exceeds CURR_LIM_SET, then U0957-4, pin 14, voltage rises and forward biases one of the D0951 diodes, which limits power.

Finally, control voltage is limited by U0956-4 and D0950. RFPA_CNTRL can rise to the control voltage limit set by R0942-4. U0965 provides protection against supply voltage transients. When transients on the A+ voltage exceed 24 volts U0965 pin 1 is pulled high thus turning on Q0954 via TX_DISABLE, R0932, U0958 disabling the control voltage to the PA first stage and momentarily turning off the transmitter. In addition, Q0900 is turned on, forward biasing one of the D0950 diodes and thus reducing the control voltage. When the voltage transient drops back below 20 volts, U0965 pin 1 goes low thus enabling the control loop and turning the transmitter on again.

3.6.3 UHF Range 2 (450-520 MHz) Band

3.6.3.1 45-Watt Transmitter

The following text discusses the 45-W transmitter.

3.6.3.1.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-29.

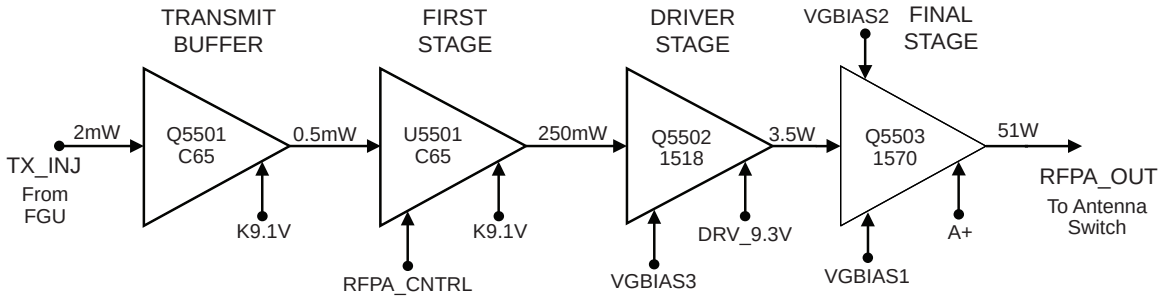

Figure 3-29. 45-Watt RF Power Amplifier (RFPA) Gain Stages (UHF Range 2)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See “3.6.3.1.3. Power Control” on page 3-39 for a detailed explanation of the power control section.

The 0.5 mW TX_INJ signal is routed to the U5501 first stage device (Pin 16, RFIN) via C5508 to an integrated, wide-band input match. U5501 is a two-stage LDMOS device with a bandpass interstage match consisting of L5503, C5507, and C5509 routed between VD1 (pin 14) and G2 (pin 11). L5502 and L5505 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U5501 stages are operated Class A and the second-stage output power is approximately 250 mW.

Driver Stage

C5566, C5516, C5518 and a transmission line form a low-pass, interstage match that transfers power to the Q5502 LDMOS transistor. R5511-R5515 provide device stability, and R5527, C5556, C5525 and R5516 supply the VGBIAS3 gate bias. L5508, C5527, R5517, E5501 and C5526 form the 9.3 V drain bias circuit. The 9.3 V drain voltage is supplied from regulator U5570. The 9.3 V supply to the driver is only present during transmit and is disabled during receive via the K9.1V signal and Q5570. Q5502 is operated Class AB and its output power is approximately 3.5 W.

Final Stage

C5559, C5560, C5535, C5538, and transmission lines form a low pass, splitter match that transfers power to the LDMOS final-stage transistor Q5503. Q5503 contains two transistors in a single package, each with it's own gate and drain lead. R5530, R5533, R5534, R5536, R5538-R5545 provide stability for Q5503. R5525, C5557, C5539 and R5520 supply the VGBIAS1 gate bias to Q5503-7 via U5504-2 pin7. R5526, C5558, C5540 and R5521 supply the VGBIAS2 gate bias to Q5503-6 via U5504-1 pin 1. Gate bias voltage to the final is adjusted dependant on the temeprature of Q5503. The output voltage from the temperature sensing IC, U5502-2, is summed via R5550 and R5555 respectively with the gate bias voltage VGBIAS1 and VGBIAS2, via R5549 and R5554 respectively. As the temeprature of the final device decreases the bias voltage applied to the gates of U5503 is reduced. L5510, C5549, R5523, E5502 and C5550 form the A+ drain bias circuit to Q5503-2 and Q5503-3. C5542-43, C5545-46, C5548, C5551-53 and transmission lines form a low -pass combiner match that transfers approximately 51 W to the antenna switch. R5535 provides stability for Q5503. Q5503 operates Class AB.

R5522 and U5503 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R5519 sets the circuit gain. U5502 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.3.1.2 Output Network (ON)

The ON consists of the antenna switch, harmonic filter, and power detector (see Figure 3-30).

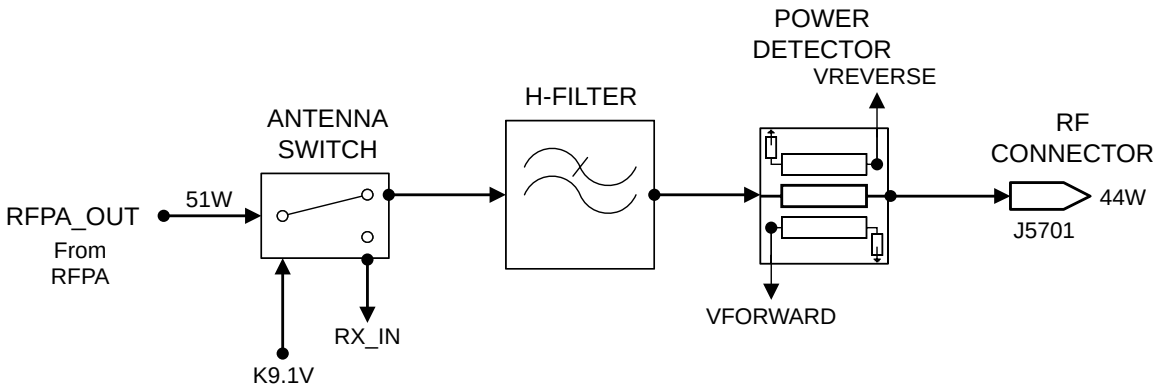

Figure 3-30. Output Network Components (UHF Range 2)

Antenna Switch

The antenna switch functions in two modes determined by the presence of K9.1V. The K9.1V switch bias is applied via L5701and C5702. When K9.1V is present, the switch is in TX mode. D5701, D5702 and D5703 are forward biased forming a low-loss path from the RFPA final stage to the harmonic filter and a 20 dB isolation path between the RFPA final stage and the RX front-end. Isolation is achieved via a quarter-wave transmission lines between D5701 - D5702 and between D5702 - D5703. C5709-10 resonates out the D5702-3 on inductance improving the isolation. When K9.1V is absent, the switch is in RX mode. D5701, D5702 and D5703 are reverse biased forming a low-loss path from the harmonic filter to the RX front-end and a 20 dB isolation path from the harmonic filter to the RFPA final stage. Isolation is achieved via the D5701 off resistance. L5702 resonates out the D5701 off capacitance improving the isolation.

Harmonic Filter

The harmonic filter is a 7-element, equal-L Zolotarev quasi-lowpass filter consisting of C5712 and C5713, C5719 thru C5721 and L5706 thru L5708. L5712, C5711 and L5713, C5714 form two shunt zeros for extra attenuation at the second harmonic. C5708 acts as a DC block between the filter and the antenna switch. The filter provides approximately 60 dB of harmonic rejection. The harmonic filter together with the antenna switch provides approximately 0.7 dB insertion loss between the transmitter power amplifier and the antenna.

Power Detector

The power detector consists of a main microstrip transmission line that transfers power from the harmonic filter to the antenna and two parallel lines that are used to detect the forward and reverse power. The forward power detection line is terminated via R5707 and R5708. RF energy coupled onto this line is rectified and filtered via D5704 and C5715 to provide a DC voltage to the power control circuitry that is proportional to the forward transmitted power level. The detected forward voltage is approximately 1.5 Vdc when the radio is putting out 44 watts. Thermister R5704 compensates for temperature changes in D5704 to maintain constant DC voltage versus detected forward power over temperature.

The reverse power detection line is terminated via R5705-06. RF energy coupled onto this line is rectified and filtered via D5705 and C5718 to provide a DC voltage to the power control circuitry that is proportional to the reverse power level reflected back from the antenna. Thermister R5712 compensates for temperature changes in D5705 to maintain constant DC voltage versus detected reverse power over temperature.

3.6.3.1.3 Power Control

The power control section is comprised of a control loop to level forward power, and protection mechanisms to reduce power to a safe level for the given environmental conditions (see Figure 3-31 on page 3-40).

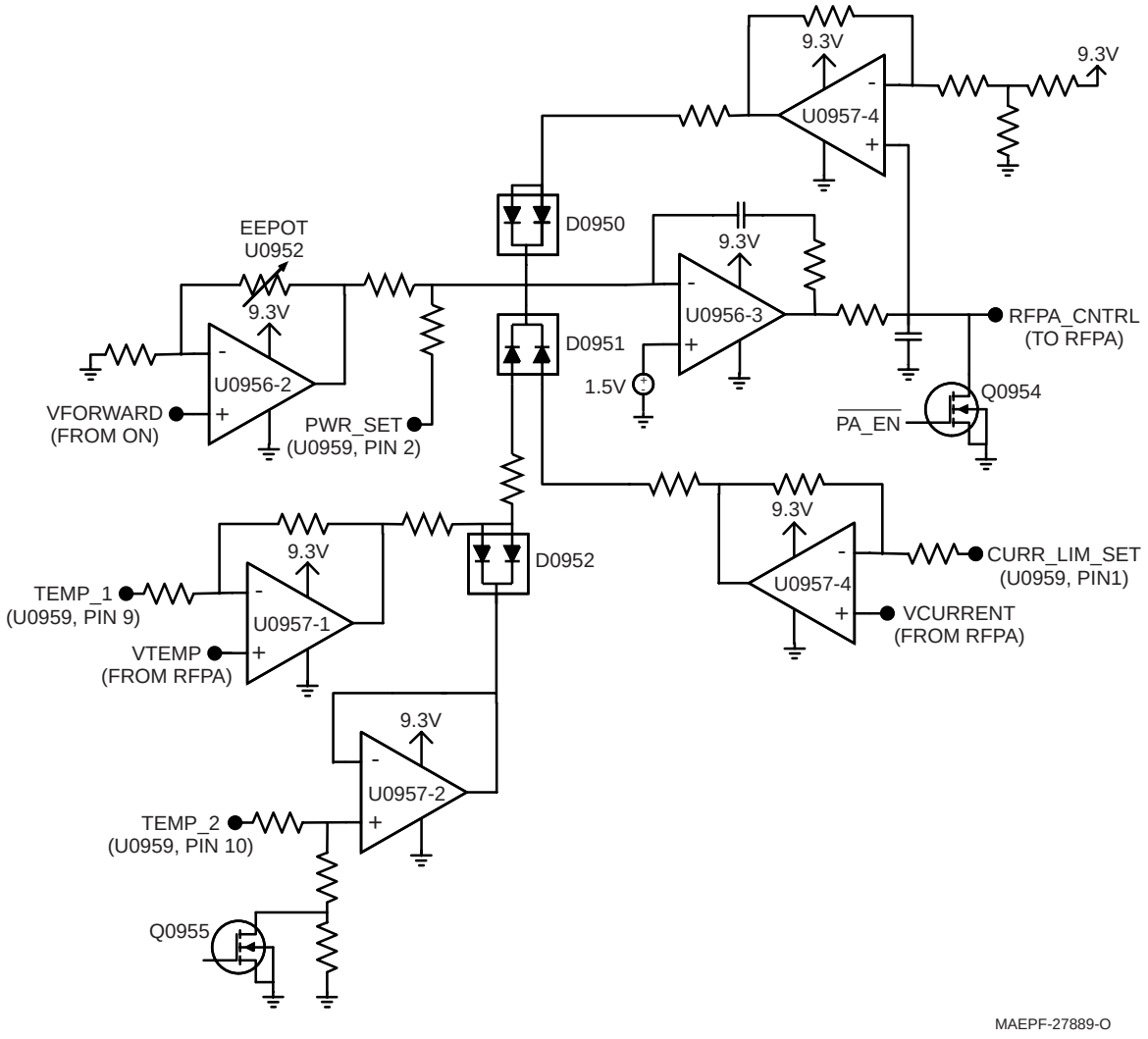

Figure 3-31. Power Control Components (UHF Range 2)

Power Control Loop

VFORWARD from the ON is buffered via the non-inverting, variable-gain stage U0956-2 whose gain is set by EPOT U0952. The proper gain is determined during power-detection calibration tuning. Buffered VFORWARD (U0956-2, Pin 7) is added to PWR_SET via R0971 and R0972 and then compared to a reference determined by R0974 and R0975. PWR_SET is supplied by the digital-to-analog converter (DAC) U0959, Pin 2. Comparator stage U0956-3 increases or decreases RFPA_CNTRL so that the voltage at U0956-3, Pin 9 in the same at the reference voltage at U0956-3, Pin 10. When the PWR_SET voltage is decreased, U0956-3 increases RFPA_CNTRL to increase VFORWARD which is proportional to forward power thus increasing the power level. When the PWR_SET voltage is increased, U0956-3 decreases RFPA_CNTRL to decrease VFORWARD, thus decreasing the power level. The microprocessor initiates the loop through U0958-1 and Q0954. Loop timing is set via software together with R0977 and C0973.

Protection Mechanisms

Final-stage temperature is sensed in the RFPA resulting in VTEMP, which is proportional to temperature. VTEMP is compared against a reference voltage TEMP_1 (U0959, pin 9) via U0957-1. When VTEMP exceeds TEMP_1, the U0957-1, pin 1, voltage increases and forward biases one of the D0951 diodes, which cuts back power. Power continues to cut back with rising temperature until the voltage level at the junction of R0978 and R0983 is high enough to forward bias D0952, thus clamping the cut back so that the radio meets its duty cycle specification while providing protection against high-temperature conditions. The clamping level is set via TEMP_2 (U0959, pin 10) and U0957-2. U0957-3 is used to sense if a high A+ battery voltage condition exists and, if it does, the Q0955 gate is biased on, which increases the clamp voltage allowing for additional power cutback for a high A+, high temperature condition.

Final-stage current is also monitored via VCURRENT, which is proportional to current. VCURRENT is compared against a reference CURR_LIM_SET (U0959, pin 1) which is tuned after power characterization. If VCURRENT exceeds CURR_LIM_SET, then U0957-4, pin 14, voltage rises and forward biases one of the D0951 diodes, which limits power.

Finally, control voltage is limited by U0956-4 and D0950. RFPA_CNTRL can rise to the control voltage limit set by R0942-4. U0965 provides protection against supply voltage transients. When transients on the A+ voltage exceed 24 volts U0965 pin 1 is pulled high thus turning on Q0954 via TX_DISABLE, R0932, U0958 disabling the control voltage to the PA first stage and momentarily turning off the transmitter. In addition, Q0900 is turned on, forward biasing one of the D0950 diodes and thus reducing the control voltage. When the voltage transient drops back below 20 volts, U0965 pin 1 goes low thus enabling the control loop and turning the transmitter on again.

3.6.4 700–800 MHz Band

3.6.4.1 35-Watt Transmitter

The following text discusses the 35-W transmitter.

3.6.4.1.1 RF Power Amplifier (RFPA)

The RFPA consists of three gain stages, which are shown in Figure 3-32.

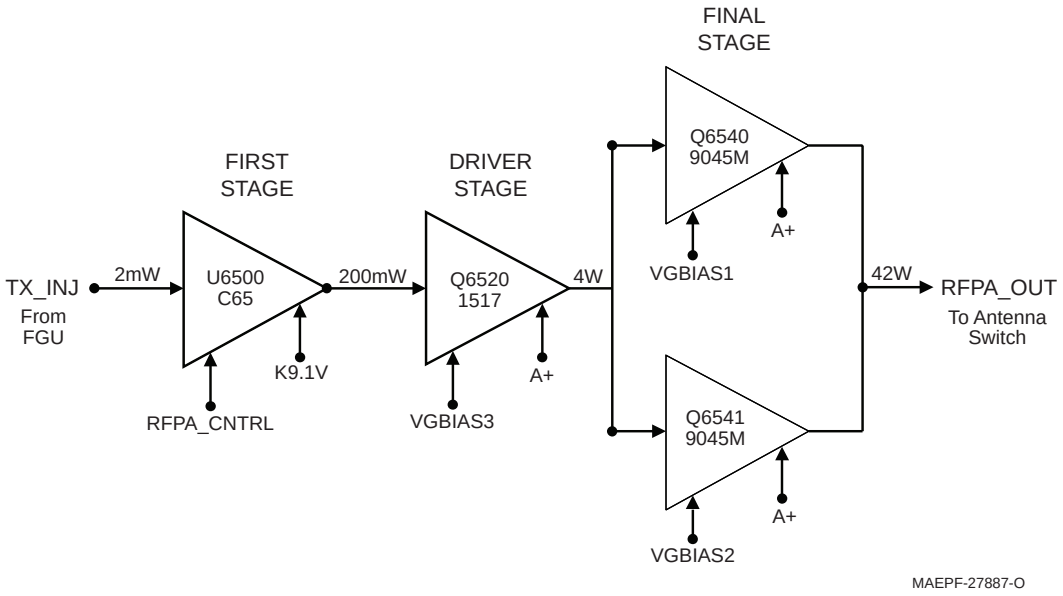

Figure 3-32. 35-Watt RF Power Amplifier (RFPA) Gain Stages (700–800 MHz)

First Stage

The RFPA first stage provides gain that is determined by the control voltage, RFPA_CNTRL. This control voltage is generated in the power control section and is a function of the final-stage output power, temperature, and current, as well as the control and A+ voltage levels. See “3.6.4.1.3. Power Control” on page 3-43 for a detailed explanation of the power control section.

The 2 mW TX_INJ signal is routed to the U6500 first-stage device (Pin 16, RFIN) via C6501 to an integrated, wide-band input match. U6500 is a two-stage LDMOS device with a bandpass interstage match consisting of L6502, C6506, and C6503 routed between VD1 (pin 14) and G2 (pin 11). L6501 and L6500 provide the K9.1V drain bias voltage for the first and second stages to VD1 (pin 14) and RFOUT1/2 (pins 6 and 7), respectively. The RFPA_CNTRL gate bias is provided to both stages internally via VCNTRL (pin 1). Both U6500 stages are operated Class A, and the second-stage output power is approximately 200 mW.

Driver Stage

C6502, C6509, C6510, C6511, and a transmission line form a low-pass, interstage match that transfers power to the Q6520 LDMOS transistor. R6521-5 provide device stability, and R6520 and C6500 supply the VGBIAS1 gate bias. L6521-2, R6526-7, and C6521-5 form the A+ drain bias circuit. Q6520 is operated Class AB, and its output power is approximately 4 W.

Final Stage

C6541-2, C6544-5, C6547-8, and transmission lines form a bandpass, splitter match that transfers power to the LDMOS final-stage transistors Q6540 and Q6541. R6550-3, R6554-7, C6565-6, and R6559-60 provide stability for Q6540 and Q6541, respectively. R6540 and C6540 supply the VGBIAS1 gate bias to Q6540. R6543 and C6558 supply the VGBIAS2 gate bias to Q6541. L6542-3, C6559-60, and R6544 form the A+ drain bias circuit.

C6549-57 and transmission lines form a low-pass, combiner match that transfers approximately 42 W to the antenna switch. Both Q6540 and Q6541 operate Class AB.

R6545-6, C6564, and U6541 comprise the final-stage, current-sense circuit that generates the VCURRENT voltage proportional to the final stage current. R6546 sets the circuit gain. U6540 generates the VTEMP voltage, which is proportional to the final-stage temperature.

3.6.4.1.2 Output Network (ON)

The ON consists of the antenna switch, harmonic filter, and power detector (see Figure 3-33).

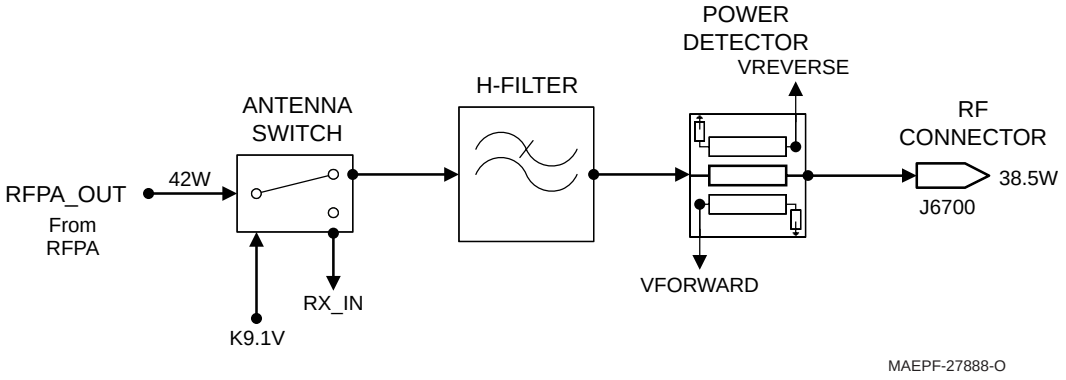

Figure 3-33. Output Network Components (700–800 MHz)

Antenna Switch

The antenna switch functions in two modes, which are determined by the presence of K9.1V. The K9.1V switch bias is applied via L6700, L6702, and C6700. When K9.1V is present, the switch is in TX mode. D6701 and D6702 are forward biased forming a low-loss path from the RFPA final stage to the harmonic filter and a 20 dB isolation path between the RFPA final stage and the RX front-end. Isolation is achieved via a quarter-wave transmission line between D6701 and D6702. C6703 resonates out the D6702 on inductance improving the isolation.

When K9.1V is absent, the switch is in RX mode. D6701 and D6702 are reverse biased forming a low-loss path from the harmonic filter to the RX front-end and a 20 dB isolation path from the harmonic filter to the RFPA final stage. Isolation is achieved via the D6701 off resistance. L6703 resonates out the D6701 off capacitance improving the isolation.

Harmonic Filter

L6720-2, C6720-1, and two open-stub transmission lines form the seven-element, low-pass harmonic filter. The filter attenuates harmonics generated by the RFPA when the antenna switch is in TX mode and provides extra selectivity when the antenna switch is in RX mode.

Power Detector

The power detector consists of two asymmetric, coupled transmission lines and detection circuitry that detects forward and reverse power. C6730-1, D6730, L6730, R6730-3, and R6735-6 form the forward-power detector (VFORWARD), which is used for power leveling. C6732-3, D6731, L6731, R6737-9, and R6733-4 form the reverse-power detector (VREVERSE). C6734-5 provides additional harmonic attenuation. R6740 provides an electrostatic discharge path to protect the RFPA final stage device.

3.6.4.1.3 Power Control

The power control section is comprised of a control loop to level forward power, and protection mechanisms to reduce power to a safe level for the given environmental conditions (see Figure 3-34 on page 3-44).

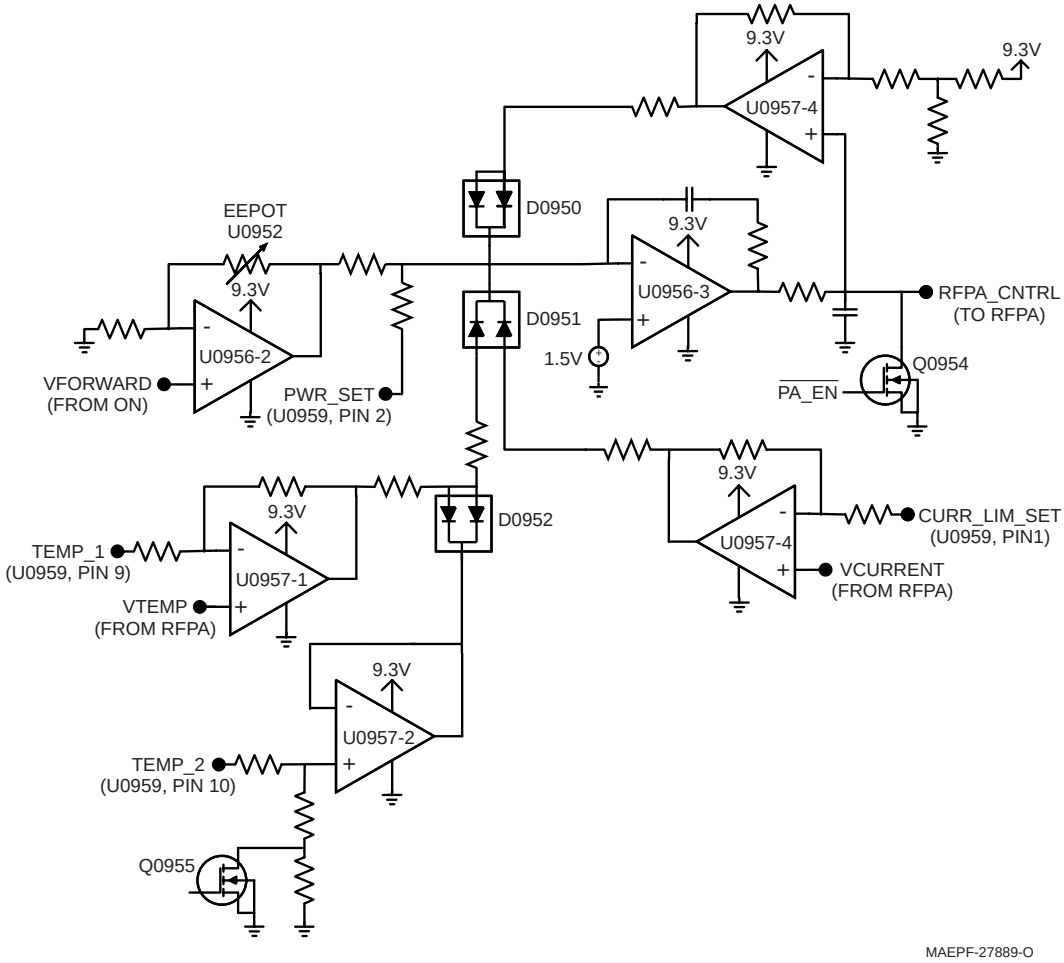

Figure 3-34. Power Control Components (700–800 MHz)

Power Control Loop

VFORWARD from the ON is buffered via the non-inverting, variable-gain stage U0956-2 whose gain is set by EPOT U0952. The proper gain is determined during power-detection calibration tuning. Buffered VFORWARD (U0956-2, Pin 7) is added to PWR_SET via R0971 and R0972 and then compared to a reference determined by R0974 and R0975. PWR_SET is supplied by the digital-to-analog converter (DAC) U0959, Pin 2. Comparator stage U0956-3 increases or decreases RFPA_CNTRL so that the voltage at U0956-3, Pin 9 in the same at the reference voltage at U0956-3, Pin 10. When the PWR_SET voltage is decreased, U0956-3 increases RFPA_CNTRL to increase VFORWARD which is proportional to forward power thus increasing the power level. When the PWR_SET voltage is increased, U0956-3 decreases RFPA_CNTRL to decrease VFORWARD, thus decreasing the power level. The microprocessor initiates the loop through U0958-1 and Q0954. Loop timing is set via software together with R0977 and C0973.

Protection Mechanisms

Final-stage temperature is sensed in the RFPA resulting in VTEMP, which is proportional to temperature. VTEMP is compared against a reference voltage TEMP_1 (U0959, pin 9) via U0957-1. When VTEMP exceeds TEMP_1, the U0957-1, pin 1, voltage increases and forward biases one of the D0951 diodes, which cuts back power. Power continues to cut back with rising temperature until the voltage level at the junction of R0978 and R0983 is high enough to forward bias D0952, thus clamping the cut back so that the radio meets its duty cycle specification while providing protection against high-temperature conditions. The clamping level is set via TEMP_2 (U0959, pin 10) and U0957-2. U0957-3 is used to sense if a high A+ battery voltage condition exists and, if it does, the Q0955 gate is biased on, which increases the clamp voltage allowing for additional power cutback for a high A+, high temperature condition.

Final-stage current is also monitored via VCURRENT, which is proportional to current. VCURRENT is compared against a reference CURR_LIM_SET (U0959, pin 1) which is tuned after power characterization. If VCURRENT exceeds CURR_LIM_SET, then U0957-4, pin 14, voltage rises and forward biases one of the D0951 diodes, which limits power.

Finally, control voltage is limited by U0956-4 and D0950. RFPA_CNTRL can rise to the control voltage limit set by R0942-4.

3.7 Frequency Generation Unit (FGU)

This section of the theory of operation provides a detailed circuit description of the frequency generation unit (FGU).

3.7.1 VHF (136-174 MHz) Band

The FGU (Figure 3-35 on page 3-46) provides the XTL 5000 radio with a 16.8 MHz reference frequency, receiver 1st local oscillator, and a modulated transmitter RF carrier that is further amplified by the power amplifier section of the radio.

The FGU consists of the following:

- Reference oscillator (Y3750)
- Low-voltage Fractional-N (LV Frac-N) synthesizer (U3751)
- Two transmitter VCOs
- Three transmitter buffer/amplifier stages
- Two Receiver VCOs
- Three receiver buffer/amplifier stages

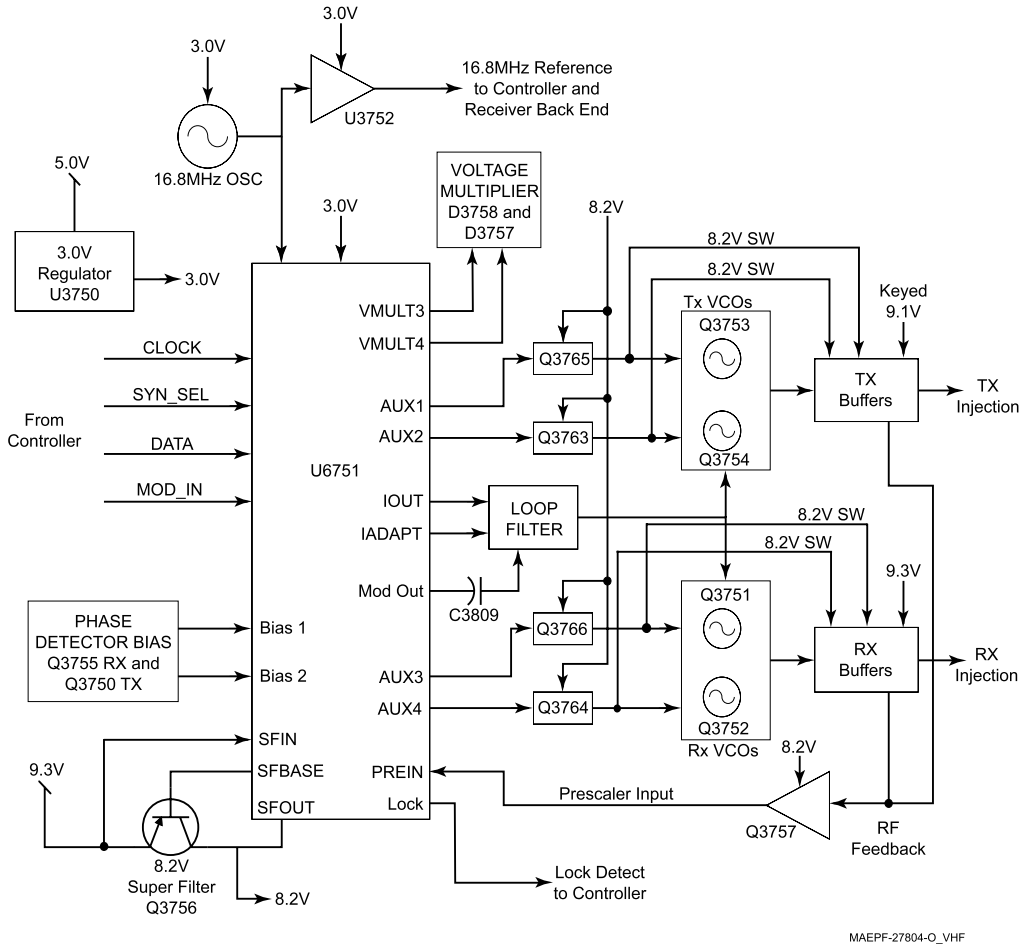

Figure 3-35. Frequency Generation Unit Block Diagram (VHF)

3.7.1.1 Reference Oscillator

The radio's frequency stability and accuracy is derived from the 16.8 MHz reference oscillator (Y3750). The 16.8 MHz reference oscillator circuitry provides a 16.8 MHz reference to the LV Frac-N (U3751), receiver backend IC (U3000), and the controller section of the XTL 5000 radio. The reference oscillator circuitry consists of the reference oscillator Y3750 and the inverter/buffer circuitry containing the active device U3752. Y3750 is a voltage-controlled, temperature-compensated crystal oscillator (VCTCXO). Circuitry internal to Y3750 compensates for frequency error over temperature. Warping of the oscillator on frequency is accomplished via a programmable DAC in the LV Frac-N. The warp voltage is present at pin 25 (WARP) of U3751 and is applied to pin 1 of Y3750. The 16.8 MHz output frequency of Y3750 is capacitor-coupled to pin 23 of the LV Frac-N (U3751) and also to the inverter/buffer stage U3752. L3754and C3824 at the output of U3752 filter the 16.8 MHz signal, and R3768 along with C3830 set the appropriate amplitude of the signal for the receiver back-end and controller sections.

3.7.1.2 LV Frac-N Synthesizer IC

The LV Frac-N IC (U3751) functions include frequency synthesis, modulation control, voltage multiplication and filtering, and auxiliary logic outputs for VCO selection.

U3751 is a mixed-mode IC containing digital and analog circuits. Separate power supply inputs are used for the various functional blocks on the IC. Inductors L3757 and L3756 provide isolation between supply pin 20 (AVDD - analog supply input) and pin 36 (DVDD - digital supply input) connected to F3.0v. This 3.0 V DC supply is provided by U3750, a 3-V regulator IC.

All programmable variables on the synthesizer IC, such as the synthesizer frequency; reference-oscillator warping; adapt-timer duration; modulation-attenuator setting; and auxiliary-control outputs, which select one of four voltage-controlled oscillators, can be programmed through a serial peripheral interface (SPI). The SPI is connected to the controller microcomputer via three programming lines, namely the data (pin 7), clock (pin 8), and the chip enable (pin 9) of U3751 (Figure 3-36).

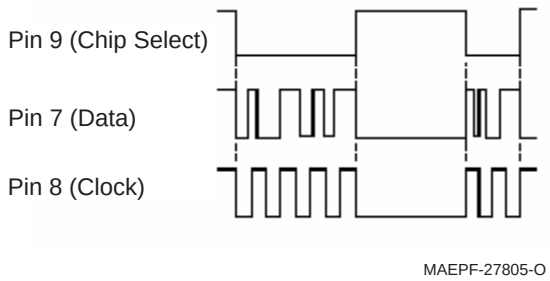

Figure 3-36. Waveform Representation During Programming of the LV Frac-N IC (VHF)

3.7.1.3 Voltage Multiplier

Pin 12 (VMULT3) and pin 11 (VMULT4) of U3751, together with diode arrays D3757 and D3758 and their associated capacitors C3763, C3764, C3765 and C3767, form the voltage multiplier. The voltage multiplier generates 12.0 Vdc from the 3.0-V supply to supply the phase detector and charge-pump output stage at pin 47 (VCP) of U3751. This voltage multiplier is basically a stacked, multiple-diode capacitor network driven by two 1.05 MHz, 180 degrees out of phase signals from pins 12 and 11 of U3751.

3.7.1.4 Superfilter

The superfilter is an active filter that provides a low-noise supply for the VCOs, receiver and transmitter injection amplifiers. Regulator U0950, located in the controller section, supplies 9.3 Vdc to the FGU section thru the filtering network consisting of L3752, C3811, C3751, and C3820. This voltage is applied to pin 30 (SFIN) of U3751 and the emitter of Q3756. The output is a superfiltered 8.2 Vdc at the junction of pin 28 (SFOUT) of U3751 and the collector of Q3756. Filtering is accomplished with capacitors C3821, C3753, and C3752 at the output of this circuit and C3823 at pin 26 of U3751.

3.7.1.5 Modulation

To support many voice, data, and signaling protocols, XTL 5000 radios must modulate the transmitter carrier frequency over a wide audio-frequency range, from less than 10 Hz up to more than 6 kHz. The LV Frac-N IC supports audio frequencies down to zero Hz by using dual-port modulation. The audio signal at pin 10 (MODIN) is internally divided into high- and low-frequency components, which modulate both the synthesizer dividers and the external VCOs through signal MODOUT (pin 41). The IC is adjusted to achieve flat modulation frequency response during transmitter modulation balance calibration using a built-in modulation attenuator.

The Digital-to-Analog Converter (DAC) IC (U0900), and switched-capacitor filter (SCF) IC (FL0900) form the interface between the radio's DSP and the analog input of the LV Frac-N IC.

3.7.1.6 Charge Pump Bias

External circuitry connected to pin 39 (Bias 2) and pin 40 (Bias 1) of U3751 determine the current that is applied to the charge-pump circuitry. During receive mode, resistors R3778, R3763, and R3758 set the current supplied to pin 40 (Bias 1). Transistor Q3755 and resistors R3779, R3756, and capacitor C3808 form a circuit that momentarily increases the current to pin 40 (Bias 1) during receiver programming of U3751. This circuit is activated by pin 46 (ADAPTSW) of U3751 during the transition of programming U3751 to frequency and effectively decreases the length of time for the synthesizer to lock on frequency. Similarly, during transmitter mode, resistors R3778, R3763, and R3776 set the current supplied to pin 39 (Bias 2). Transistor Q3750 and resistors R3759, R3776, and capacitor C3825 form a circuit that momentarily increases the current to pin 39 (Bias 2) during transmitter programming of U3751.

3.7.1.7 Loop Filter

The loop filter operates in synchronization with the phase detector of U3751 in two modes, normal and adapt. In normal mode, the loop filter forms a third-order loop filter consisting of components R3765, R3773, R3770, C3833, C3810, C3834, C3855 to C3861 and C3881 to C3883.

Pin 43 (IOUT) of U3751 provides the charge-pump current for steering of the control voltage line to the VCOs. During normal mode, pin 45 (IADAPT) is set to a high impedance and has no effect on the loop filter. When U3751 is programmed to a new frequency, the IC is initially operated in adapt mode. In this mode the loop filter is reconfigured for a wider bandwidth allowing the synthesizer to lock faster. The charge-pump output is supplied through pin 45 (IADAPT) in this mode, and this reconfigures the loop filter to behave like a second-order filter.

3.7.1.8 Lock Detect

Lock status of the synthesizer loop is provided to the microprocessor by pin 4 (LOCK) of U3751. A high level (3.0 Vdc) indicates that the loop is stable. A low voltage indicates that the loop is not locked and will result in a Fail 001 to be displayed on the control head display.

3.7.1.9 Transmitter Injection

The transmit (TX) injection string consists of three amplifier stages (Q3760, Q3759, and Q3758) whose main purpose is to maintain a constant output to drive the RF power amplifier and supply the TX feedback signal to the FGU synthesizer loop. The first two stages are powered by the superfiltered 8.2 Vdc, which is decreased by 0.7 Vdc via the dual diode D3750, resulting in a 7.5 Vdc supply. The third stage is powered by the keyed 9.1 Vdc and the TX injection string is on only with keyed 9.1 Vdc activated during transmit mode. The TX VCO output is attenuated 3 dB via resistors R3840, R3833, and R3839. This output is coupled to the first-stage amplifier Q3760, further attenuated 3 dB via resistors R3803, R3809, and R3803, and then coupled to the second-stage amplifier Q3759. This output is tapped to supply the TX feedback signal to the synthesizer prescaler, and the balance is further attenuated 5 dB via resistors R3818, R3823, and R3824. This output is coupled to the third- stage amplifier Q3758, further attenuated 3 dB via resistors R3858, R3863, and R3859, routed to the 7-pole Cow Chebychev low-pass filter C3917 through C3921, L3785, and L3787 in order to attenuate harmonics. The output is, again, attenuated 3 dB via resistors R3842, R3834, and R3841 and coupled to the input of the RF power amplifier section. The five sets of resistive attenuators provide increased isolation between the TX VCO and RF power amplifier.

3.7.1.10 Receiver Injection

The receiver (RX) injection string is a three-stage amplifier that supplies the RX feedback signal to the FGU synthesizer loop and supplies the first local oscillator (LO) signal to the RX front-end mixer. The RX VCO output is attenuated 3 dB via resistors R3825 through R3827 to increase isolation. This buffered signal is amplified by the first-stage amplifier Q3761, which is supplied by the 8.2-V superfilter for a gain of approximately 6 dB. Resistors R3790, R3798, R3800, and R3801 bias Q3761. L3774 serves as a choke inductor; C3779 and C3868 are added for filtering. The output of Q3761 is attenuated 9.5 dB via resistors R3854, R3865, and R3855. This output is coupled to Q3769 which gain of approximately 3 dB. The output of Q3769 is split into two paths. The first path feeds back to the synthesizer prescaler through blocking capacitor C3913. The second path, which supplies the LO signal to the RX front-end mixer, is attenuated 3 dB via resistors R3857, R3864, and R3856 to increase isolation. This buffered signal is amplified by the second-stage amplifier Q3762, which is supplied by the 9.3-V regulator for a gain of approximately 15 dB. Resistors R3843, R3851, and R3852 biases Q3762. L3783 serves as a choke inductor; C3873, C3870, and C3925 are added for filtering. The output of Q3762 is passed through blocking capacitor C3759, then, routed to C3804, L3781, C3786, and L3782 which form a low pass filter and attenuated 1 dB via resistors R3821, R3794, and R3802 to increase isolation and supply approximately 20 dBm to the LO port of the mixer.

3.7.1.11 Transmitter VCOs

Transmitter frequencies are generated from two external, discrete, Colpits VCOs, low band (136-155 MHz) and high band (155-174 MHz), based on Q3753 and Q3754 respectively. The VCOs are switched On and Off by transistors Q3765 and Q3763, which are controlled by the Frac-N outputs AUX1 and AUX2 respectively when turned high.

3.7.1.12 Receiver VCOs

The receiver first local oscillator frequencies are generated from two external, discrete, Colpits VCOs, low band (245.65-264.65) and high band (264.65-283.65), based on Q3751 and Q3752 respectively. The VCOs are switched On and Off by transistors Q3766 and Q3764, which are controlled by the Frac-N outputs AUX3 and AUX4 respectively when turned high.

3.7.1.13 Prescaler Feedback

RF feedback for the synthesizer loop is provided by prescaler amplifier Q3757. Feedback from both the transmitter and receiver injection strings are coupled to this amplifier through resistor networks that both balance and attenuate the levels prior to amplification by Q3757. The output of Q3757 is coupled to U3751 at pin 32 (PREIN), which is the prescaler input for the synthesizer.

3.7.2 UHF Range 1 (380–470 MHz) Band

The FGU (Figure 3-37 on page 3-50) provides the XTL 5000 radio with a 16.8 MHz reference frequency, receiver 1st local oscillator, and a modulated transmitter RF carrier that is further amplified by the power amplifier section of the radio.

The FGU consists of the following:

- Reference oscillator (Y5750)
- Low-voltage Fractional-N (LV Frac-N) synthesizer (U5752)
- Three receiver voltage-controlled oscillators (VCOs)
- Two transmitter VCOs
- Three receiver LO amplifiers (Q5904, Q5902 and Q5906)
- Two transmitter injection amplifiers (Q5828, and Q5829)

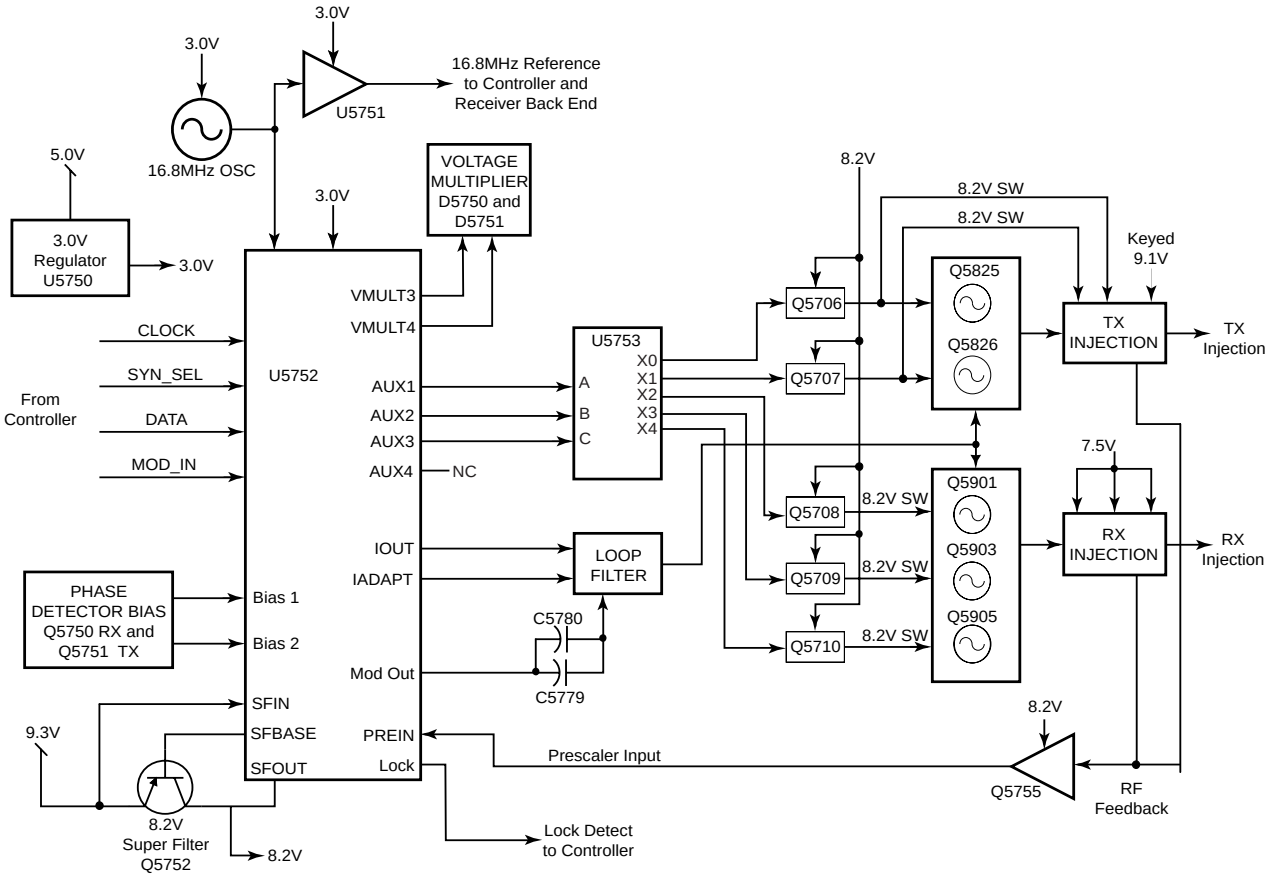

Figure 3-37. Frequency Generation Unit Block Diagram (UHF Range 1)

3.7.2.1 Reference Oscillator

The radio's frequency stability and accuracy is derived from the 16.8 MHz reference oscillator (Y5750). The 16.8 MHz reference oscillator circuitry provides a 16.8 MHz reference to the LV Frac-N (U5752), receiver back-end IC (U5002), and the controller section of the XTL 5000 radio. The reference oscillator circuitry consists of the reference oscillator Y5750 and the inverter/buffer circuitry containing the active device U5751. Y5750 is a voltage-controlled, temperature-compensated crystal oscillator (VCTCXO). Circuitry internal to Y5750 compensates for frequency error over temperature. Warping of the oscillator on frequency is accomplished via a programmable DAC in the LV Frac-N. The warp voltage is present at pin 25 (WARP) of U5752 and is applied to pin 1 of Y5750. The 16.8 MHz output frequency of Y5750 is capacitor-coupled to pin 23 of the LV Frac-N (U5752) and also to the inverter/buffer stage U5751. L5753 and C5768 at the output of U5751 filter the 16.8 MHz signal, and R5768 along with C5763 set the appropriate amplitude of the signal for the receiver back-end and controller sections.

3.7.2.2 LV Frac-N Synthesizer IC

The LV Frac-N IC (U5752) functions include frequency synthesis, modulation control, voltage multiplication and filtering, and auxiliary logic outputs for VCO selection.

U5752 is a mixed-mode IC containing digital and analog circuits. Separate power supply inputs are used for the various functional blocks on the IC. Inductors L5755 and L5756 provide isolation between supply pin 20 (AVDD - analog supply input) and pin 36 (DVDD - digital supply input) connected to F3.0v. This 3.0 V DC supply is provided by U5750, a 3-V regulator IC.

All programmable variables on the synthesizer IC, such as the synthesizer frequency; reference-oscillator warping; adapt-timer duration; modulation-attenuator setting; and auxiliary-control outputs, which select one of five voltage-controlled oscillators, can be programmed through a serial peripheral interface (SPI). The SPI is connected to the controller microcomputer via three programming lines, namely the data (pin 7), clock (pin 8), and the chip enable (pin 9) of U5752 (Figure 3-38).

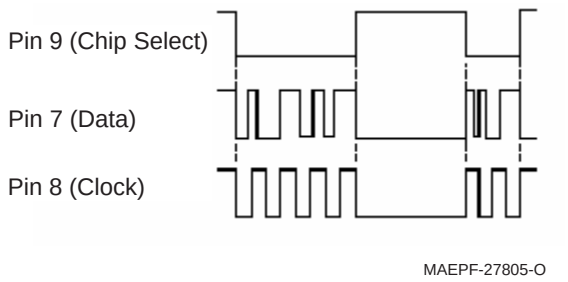

Figure 3-38. Waveform Representation During Programming of the LV Frac-N IC (UHF Range 1)

3.7.2.3 Voltage Multiplier

Pin 12 (VMULT3) and pin 11 (VMULT4) of U5752, together with diode arrays D5750 and D5751 and their associated capacitors C5775, C5776, C5777 and C5778, form the voltage multiplier. The voltage multiplier generates 13.4 Vdc from the 5.0-V supply to supply the phase detector and charge-pump output stage at pin 47 (VCP) of U5752. This voltage multiplier is basically a stacked, multiple-diode capacitor network driven by two 1.05 MHz, 180 degrees out of phase signals from pins 12 and 11 of U5752.

3.7.2.4 Superfilter

The superfilter is an active filter that provides a low-noise supply for the VCOs, receiver and transmitter injection amplifiers. Regulator U0950, located in the controller section, supplies 9.3 Vdc to the FGU section thru the filtering network consisting of L5750, C5751, C5753, and C5755. This voltage is applied to pin 30 (SFIN) of U5752 and the emitter of Q5752. The output is a superfiltered 8.2 Vdc at the junction of pin 28 (SFOUT) of U5752 and the collector of Q5752. Filtering is accomplished with capacitors C5766, C5769, and C5772 at the output of this circuit and C5770 at pin 26 of U5752.

3.7.2.5 Modulation

To support many voice, data, and signaling protocols, XTL 5000 radios must modulate the transmitter carrier frequency over a wide audio-frequency range, from less than 10 Hz up to more than 6 kHz. The LV Frac-N IC supports audio frequencies down to zero Hz by using dual-port modulation. The audio signal at pin 10 (MODIN) is internally divided into high- and low-frequency components, which modulate both the synthesizer dividers and the external VCOs through signal MODOUT (pin 41). The IC is adjusted to achieve flat modulation frequency response during transmitter modulation balance calibration using a built-in modulation attenuator.

The Digital-to-Analog Converter (DAC) IC (U0900), and switched-capacitor filter (SCF) IC (FL0900) form the interface between the radio's DSP and the analog input of the LV Frac-N IC.

3.7.2.6 Charge Pump Bias

External circuitry connected to pin 39 (Bias 2) and pin 40 (Bias 1) of U5752 determine the current that is applied to the charge-pump circuitry. During receive mode, resistors R5754, R5759, and R5765 set the current supplied to pin 40 (Bias 1). Transistor Q5750 and resistors R5752, R5753, and capacitor C5759 form a circuit that momentarily increases the current to pin 40 (Bias 1) during receiver programming of U5752. This circuit is activated by pin 46 (ADAPTSW) of U5752 during the transition of programming U5752 to frequency and effectively decreases the length of time for the synthesizer to lock on frequency. Similarly, during transmitter mode, resistors R5764, R5759, and R5753 set the current supplied to pin 39 (Bias 2). Transistor Q5752 and resistors R5767, R5764, and capacitor C5762 form a circuit that momentarily increases the current to pin 39 (Bias 2) during transmitter programming of U5752.

3.7.2.7 Loop Filter

The loop filter operates in synchronization with the phase detector of U5752 in two modes, normal and adapt. In normal mode, the loop filter forms a third-order loop filter consisting of components R5772, R5774, R5775, C5781 to C5787, C5790 to C5792, and C5809 to C5812.

Pin 43 (IOUT) of U5752 provides the charge-pump current for steering of the control voltage line to the VCOs. During normal mode, pin 45 (IADAPT) is set to a high impedance and has no effect on the loop filter. When U5752 is programmed to a new frequency, the IC is initially operated in adapt mode. In this mode the loop filter is reconfigured for a wider bandwidth allowing the synthesizer to lock faster. The charge-pump output is supplied through pin 45 (IADAPT) in this mode, and this reconfigures the loop filter to behave like a second-order filter.

3.7.2.8 Lock Detect

Lock status of the synthesizer loop is provided to the microprocessor by pin 4 (LOCK) of U5752. A high level (3.0 Vdc) indicates that the loop is stable. A low voltage indicates that the loop is not locked and will result in a Fail 001 to be displayed on the control head display.

3.7.2.9 Transmitter Injection

The transmit (TX) injection string consists of three amplifier stages (Q5828, Q5829, and Q5501) whose main purpose is to maintain a constant output to drive the RF power amplifier chain and supply the TX feedback signal to the FGU synthesizer loop. The first two stages are powered by the superfiltered 8.2 Vdc, which is decreased by 0.7 Vdc via the dual diode D5833, resulting in a 7.5 Vdc supply. The third stage is powered by the keyed 9.1 Vdc and the TX injection string is on only with keyed 9.1 Vdc activated during transmit mode.

The output of the second stage amplifier Q5829 is tapped via capacitor C5863 to supply the TX feedback signal to the synthesizer prescalar via the amplifier Q5755.

3.7.2.10 Receiver Injection

The receiver (RX) injection string is a four-stage amplifier that supplies the RX feedback signal to the FGU synthesizer loop and supplies the first local oscillator (LO) signal to the RX front-end mixer. Each RX VCO output is attenuated via resistive pads to increase isolation. The VCO signals are buffered by the RX injection amplifier string Q5904, Q5902 and Q5906. The output of Q5906 is tapped via C5957 and fed back to the synthesizer prescaler through amplifier Q5755. The main path at the output of Q5906 is amplified by U5303 to a level of 24 dBm to provide the first LO signal to the RX front end mixer in the receiver chain.

3.7.2.11 Transmitter VCOs

Transmitter frequencies are generated from two VCOs, Q5825 and Q5826.

- Q5825 supplies frequencies in the range 380 MHz up to (but not including) 425 MHz.
- Q5826 supplies frequencies in the range from 425 MHz to 470 MHz.

3.7.2.12 Receiver VCOs

Receiver first local-oscillator frequencies are generated from three VCOs, Q5901, Q5903 and Q5905.

- Q5901 supplies frequencies in the range 489.65 MHz up to (but not including) 519.65 MHz.
- Q5903 supplies frequencies in the range 519.65 MHz up to (but not including) 549.65 MHz.
- Q5905 supplies frequencies in the range 549.65 MHz up to 579.65 MHz.

The RX VCOs operate at frequencies which are 109.65 MHz higher than the radio channel selected frequency since the receiver is high side injected, and the first IF frequency is 109.65 MHz.

The five VCOs are selected by the following pattern of logic levels on the AUX pins from the synthesizer chip U5752 (Table 3-11):

Table 3-11. VCO AUX Pin Logic UHF Range 1

VCO	AUX1	AUX2	AUX3
RX VCO Q5901	0	1	0
RX VCO Q5903	1	1	0
RX VCO Q5905	0	0	1
TX VCO Q5825	0	0	0
TX VCO Q5826	1	0	0

3.7.2.13 Prescaler Feedback

RF feedback for the synthesizer loop is provided by prescaler amplifier Q5755. Feedback from both the transmitter and receiver injection strings are coupled to this amplifier through capacitors C5863 and C5957. The output of Q5755 is coupled to U5752 at pin 32 (PREIN), which is the prescaler input for the synthesizer.

3.7.3 UHF Range 2 (450–520 MHz) Band

The FGU (Figure 3-39) provides the XTL 5000 radio with a 16.8 MHz reference frequency, receiver 1st local oscillator, and a modulated transmitter RF carrier that is further amplified by the power amplifier section of the radio.

The FGU consists of the following:

- Reference oscillator (Y5750)
- Low-voltage Fractional-N (LV Frac-N) synthesizer (U5752)
- Three receiver voltage-controlled oscillators (VCOs)
- Two transmitter VCOs
- Three receiver LO amplifiers (Q5904, Q5902 and Q5906)
- Two transmitter injection amplifiers (Q5828, and Q5829)

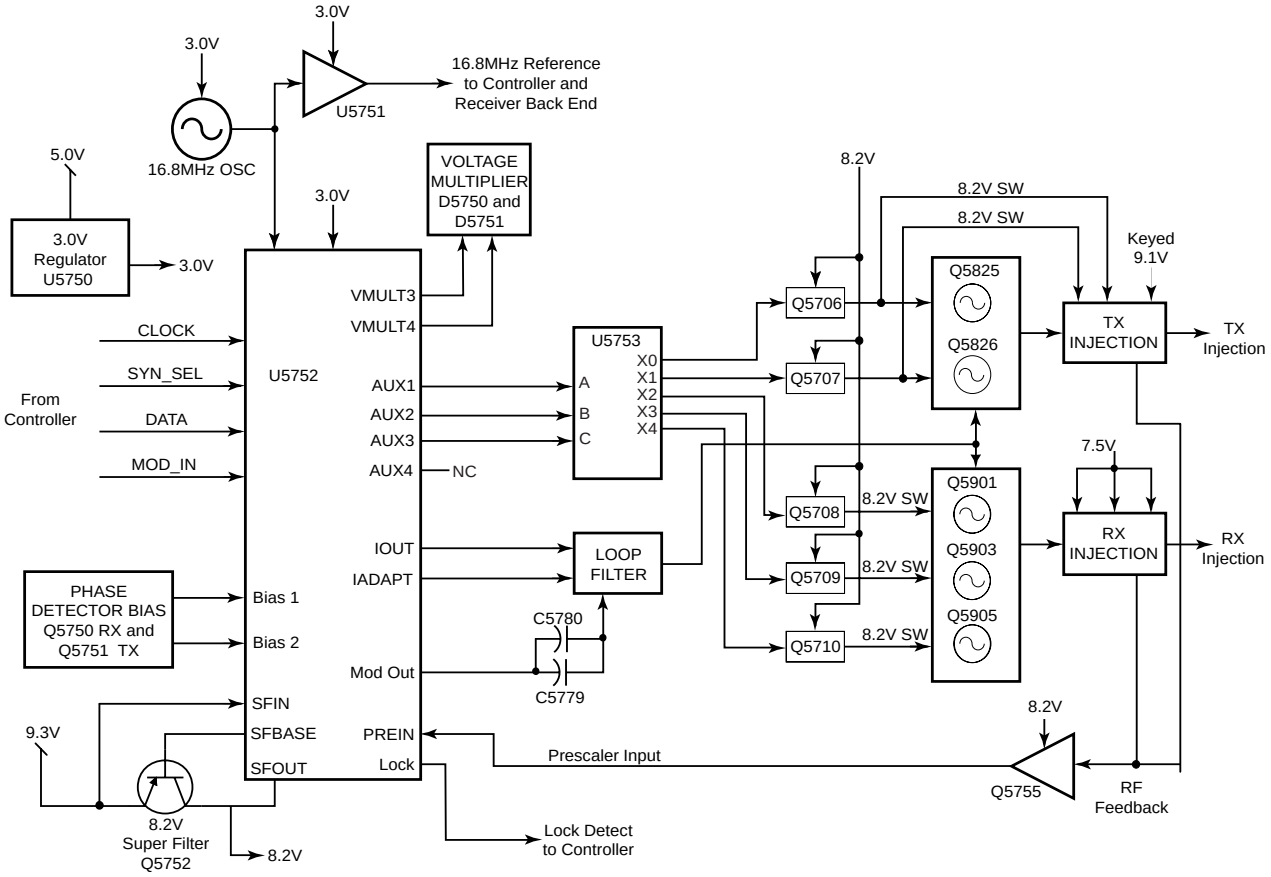

Figure 3-39. Frequency Generation Unit Block Diagram (UHF Range 2)

3.7.3.1 Reference Oscillator

The radio's frequency stability and accuracy is derived from the 16.8 MHz reference oscillator (Y5750). The 16.8 MHz reference oscillator circuitry provides a 16.8 MHz reference to the LV Frac-N (U5752), receiver back-end IC (U5002), and the controller section of the XTL 5000 radio. The reference oscillator circuitry consists of the reference oscillator Y5750 and the inverter/buffer circuitry containing the active device U5751. Y5750 is a voltage-controlled, temperature-compensated crystal oscillator (VCTCXO). Circuitry internal to Y5750 compensates for frequency error over temperature. Warping of the oscillator on frequency is accomplished via a programmable DAC in the LV Frac-N. The warp voltage is present at pin 25 (WARP) of U5752 and is applied to pin 1 of Y5750. The 16.8 MHz output frequency of Y5750 is capacitor-coupled to pin 23 of the LV Frac-N (U5752) and also to the inverter/buffer stage U5751. L5753 and C5768 at the output of U5751 filter the 16.8 MHz signal, and R5768 along with C5763 set the appropriate amplitude of the signal for the receiver back-end and controller sections.

3.7.3.2 LV Frac-N Synthesizer IC

The LV Frac-N IC (U5752) functions include frequency synthesis, modulation control, voltage multiplication and filtering, and auxiliary logic outputs for VCO selection.

U5752 is a mixed-mode IC containing digital and analog circuits. Separate power supply inputs are used for the various functional blocks on the IC. Inductors L5755 and L5756 provide isolation between supply pin 20 (AVDD - analog supply input) and pin 36 (DVDD - digital supply input) connected to F3.0v. This 3.0 V DC supply is provided by U5750, a 3-V regulator IC.

All programmable variables on the synthesizer IC, such as the synthesizer frequency; reference-oscillator warping; adapt-timer duration; modulation-attenuator setting; and auxiliary-control outputs, which select one of five voltage-controlled oscillators, can be programmed through a serial peripheral interface (SPI). The SPI is connected to the controller microcomputer via three programming lines, namely the data (pin 7), clock (pin 8), and the chip enable (pin 9) of U5752 (Figure 3-40).

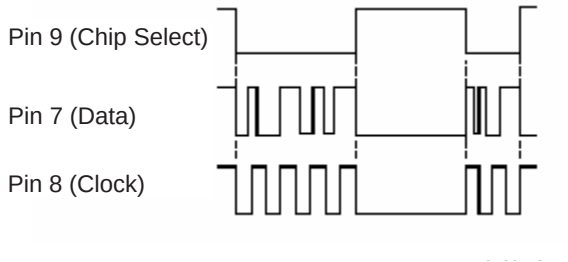

Figure 3-40. Waveform Representation During Programming of the LV Frac-N IC (UHF Range 2)

3.7.3.3 Voltage Multiplier

Pin 12 (VMULT3) and pin 11 (VMULT4) of U5752, together with diode arrays D5750 and D5751 and their associated capacitors C5775, C5776, C5777 and C5778, form the voltage multiplier. The voltage multiplier generates 13.4 Vdc from the 5.0-V supply to supply the phase detector and charge-pump output stage at pin 47 (VCP) of U5752. This voltage multiplier is basically a stacked, multiple-diode capacitor network driven by two 1.05 MHz, 180 degrees out of phase signals from pins 12 and 11 of U5752.

3.7.3.4 Superfilter

The superfilter is an active filter that provides a low-noise supply for the VCOs, receiver and transmitter injection amplifiers. Regulator U0950, located in the controller section, supplies 9.3 Vdc to the FGU section thru the filtering network consisting of L5750, C5751, C5753, and C5755. This voltage is applied to pin 30 (SFIN) of U5752 and the emitter of Q5752. The output is a superfiltered 8.2 Vdc at the junction of pin 28 (SFOUT) of U5752 and the collector of Q5752. Filtering is accomplished with capacitors C5766, C5769, and C5772 at the output of this circuit and C5770 at pin 26 of U5752.

3.7.3.5 Modulation

To support many voice, data, and signaling protocols, XTL 5000 radios must modulate the transmitter carrier frequency over a wide audio-frequency range, from less than 10 Hz up to more than 6 kHz. The LV Frac-N IC supports audio frequencies down to zero Hz by using dual-port modulation. The audio signal at pin 10 (MODIN) is internally divided into high- and low-frequency components, which modulate both the synthesizer dividers and the external VCOs through signal MODOUT (pin 41). The IC is adjusted to achieve flat modulation frequency response during transmitter modulation balance calibration using a built-in modulation attenuator.

The Digital-to-Analog Converter (DAC) IC (U0900), and switched-capacitor filter (SCF) IC (FL0900) form the interface between the radio's DSP and the analog input of the LV Frac-N IC.

3.7.3.6 Charge Pump Bias

External circuitry connected to pin 39 (Bias 2) and pin 40 (Bias 1) of U5752 determine the current that is applied to the charge-pump circuitry. During receive mode, resistors R5754, R5759, and R5765 set the current supplied to pin 40 (Bias 1). Transistor Q5750 and resistors R5752, R5753, and capacitor C5759 form a circuit that momentarily increases the current to pin 40 (Bias 1) during receiver programming of U5752. This circuit is activated by pin 46 (ADAPTSW) of U5752 during the transition of programming U5752 to frequency and effectively decreases the length of time for the synthesizer to lock on frequency. Similarly, during transmitter mode, resistors R5764, R5759, and R5753 set the current supplied to pin 39 (Bias 2). Transistor Q5752 and resistors R5767, R5764, and capacitor C5762 form a circuit that momentarily increases the current to pin 39 (Bias 2) during transmitter programming of U5752.

3.7.3.7 Loop Filter

The loop filter operates in synchronization with the phase detector of U5752 in two modes, normal and adapt. In normal mode, the loop filter forms a third-order loop filter consisting of components R5772, R5774, R5775, C5781 to C5787, C5790 to C5792, and C5809 to C5812.

Pin 43 (IOUT) of U5752 provides the charge-pump current for steering of the control voltage line to the VCOs. During normal mode, pin 45 (IADAPT) is set to a high impedance and has no effect on the loop filter. When U5752 is programmed to a new frequency, the IC is initially operated in adapt mode. In this mode the loop filter is reconfigured for a wider bandwidth allowing the synthesizer to lock faster. The charge-pump output is supplied through pin 45 (IADAPT) in this mode, and this reconfigures the loop filter to behave like a second-order filter.

3.7.3.8 Lock Detect

Lock status of the synthesizer loop is provided to the microprocessor by pin 4 (LOCK) of U5752. A high level (3.0 Vdc) indicates that the loop is stable. A low voltage indicates that the loop is not locked and will result in a Fail 001 to be displayed on the control head display.

3.7.3.9 Transmitter Injection

The transmit (TX) injection string consists of three amplifier stages (Q5828, Q5829, and Q5501) whose main purpose is to maintain a constant output to drive the RF power amplifier chain and supply the TX feedback signal to the FGU synthesizer loop. The first two stages are powered by the superfiltered 8.2 Vdc, which is decreased by 0.7 Vdc via the dual diode D5833, resulting in a 7.5 Vdc supply. The third stage is powered by the keyed 9.1 Vdc and the TX injection string is on only with keyed 9.1 Vdc activated during transmit mode.

The output of the second stage amplifier Q5829 is tapped via capacitor C5863 to supply the TX feedback signal to the synthesizer prescalar via the amplifier Q5755.

3.7.3.10 Receiver Injection

The receiver (RX) injection string is a four-stage amplifier that supplies the RX feedback signal to the FGU synthesizer loop and supplies the first local oscillator (LO) signal to the RX front-end mixer. Each RX VCO output is attenuated via resistive pads to increase isolation. The VCO signals are buffered by the RX injection amplifier string Q5904, Q5902 and Q5906. The output of Q5906 is tapped via C5957 and fed back to the synthesizer prescaler through amplifier Q5755. The main path at the output of Q5906 is amplified by U5303 to a level of 24 dBm to provide the first LO signal to the RX front end mixer in the receiver chain.

3.7.3.11 Transmitter VCOs

Transmitter frequencies are generated from two VCOs, Q5825 and Q5826.

- Q5826 supplies frequencies in the range 450 MHz up to (but not including) 485 MHz.
- Q5825 supplies frequencies in the range from 485 MHz to 520 MHz.

3.7.3.12 Receiver VCOs

Receiver first local-oscillator frequencies are generated from three VCOs, Q5901, Q5903 and Q5905.

- Q5905 supplies frequencies in the range 559.65 MHz up to (but not including) 582.65 MHz.
- Q5903 supplies frequencies in the range 582.65 MHz up to (but not including) 605.65 MHz.
- Q5901 supplies frequencies in the range 605.65 MHz up to 629.65 MHz.

The RX VCOs operate at frequencies which are 109.65 MHz higher than the radio channel selected frequency since the receiver is high side injected, and the first IF frequency is 109.65 MHz.

The five VCOs are selected by the following pattern of logic levels on the AUX pins from the synthesizer chip U5752 (Table 3-12):

Table 3-12. VCO AUX Pin Logic UHF Range 2

VCO	AUX1	AUX2	AUX3
RX VCO Q5905	0	0	1
RX VCO Q5903	1	1	0
RX VCO Q5901	0	1	0
TX VCO Q5826	1	0	0
TX VCO Q5825	0	0	0

3.7.3.13 Prescaler Feedback

RF feedback for the synthesizer loop is provided by prescaler amplifier Q5755. Feedback from both the transmitter and receiver injection strings are coupled to this amplifier through capacitors C5863 and C5957. The output of Q5755 is coupled to U5752 at pin 32 (PREIN), which is the prescaler input for the synthesizer.

3.7.4 700–800 MHz Band

The FGU (Figure 3-41) provides the XTL 5000 radio with a 16.8 MHz reference frequency, receiver 1st local oscillator, and a modulated transmitter RF carrier that is further amplified by the power amplifier section of the radio.

The FGU consists of the following:

- Reference oscillator (Y6750)
- Low-voltage Fractional-N (LV Frac-N) synthesizer (U6751)
- Two receiver voltage-controlled oscillators (VCOs) contained in U6755
- Two transmitter VCOs contained in U6754
- Two receiver LO amplifiers (Q6762 and Q6763)
- Three transmitter injection amplifiers (Q6764, Q6765 and Q6766)

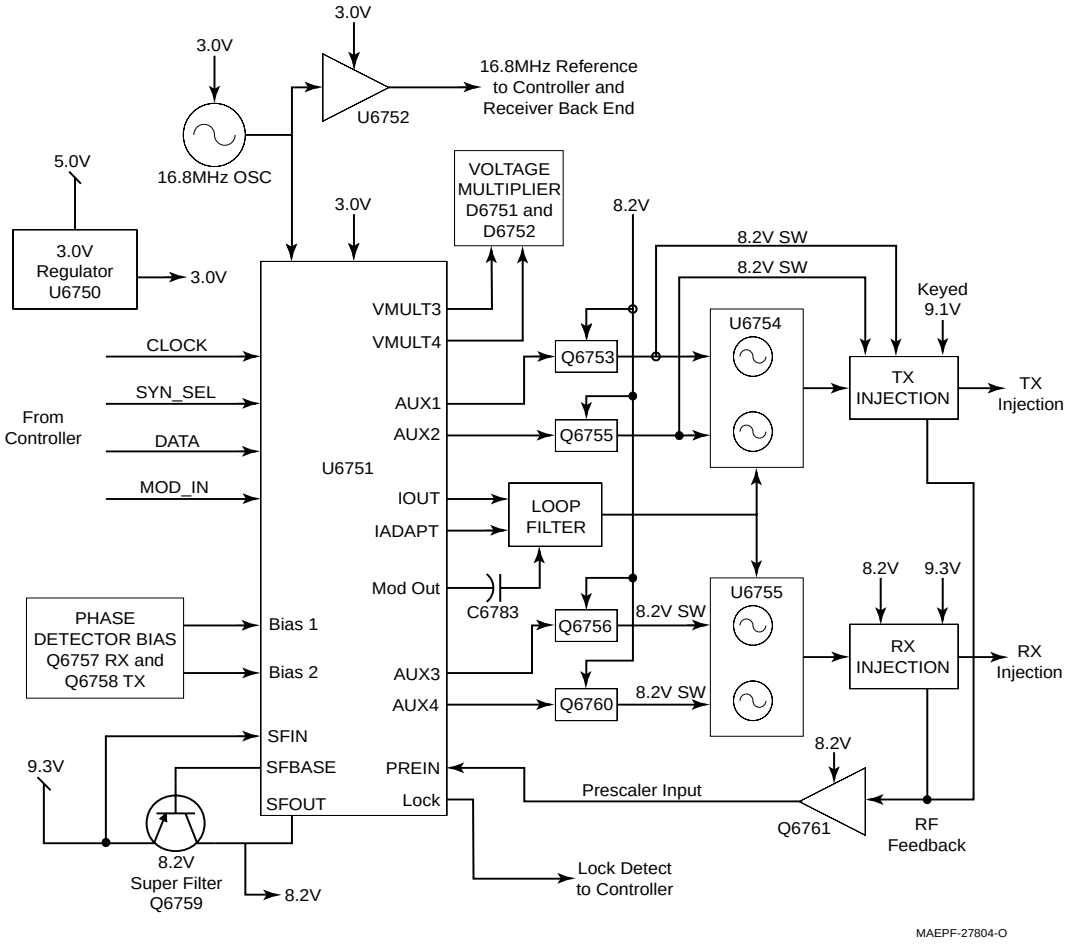

Figure 3-41. Frequency Generation Unit Block Diagram (700–800 MHz)

3.7.4.1 Reference Oscillator

The radio's frequency stability and accuracy is derived from the 16.8 MHz reference oscillator (Y6750). The 16.8 MHz reference oscillator circuitry provides a 16.8 MHz reference to the LV Frac-N (U6751), receiver back-end IC (U6000), and the controller section of the XTL 5000 radio. The reference oscillator circuitry consists of the reference oscillator Y6750 and the inverter/buffer circuitry containing the active device U6752. Y6750 is a voltage-controlled, temperature-compensated crystal oscillator (VCTCXO). Circuitry internal to Y6750 compensates for frequency error over temperature. Warping of the oscillator on frequency is accomplished via a programmable DAC in the LV Frac-N. The warp voltage is present at pin 25 (WARP) of U6751 and is applied to pin 4 of Y6750. The 16.8 MHz output frequency of Y6750 is capacitor-coupled to pin 24 of the LV Frac-N (U6751) and also to the inverter/buffer stage U6752. L6756 and C6755 at the output of U6752 filter the 16.8 MHz signal, and R6757 along with C6759 set the appropriate amplitude of the signal for the receiver back-end and controller sections.

3.7.4.2 LV Frac-N Synthesizer IC

The LV Frac-N IC (U6751) functions include frequency synthesis, modulation control, voltage multiplication and filtering, and auxiliary logic outputs for VCO selection.

U6751 is a mixed-mode IC containing digital and analog circuits. Separate power supply inputs are used for the various functional blocks on the IC. Inductors L6752 and L6753 provide isolation between supply pin 20 (AVDD - analog supply input) and pin 36 (DVDD - digital supply input) connected to F3.0v. This 3.0 V DC supply is provided by U6750, a 3-V regulator IC.

All programmable variables on the synthesizer IC, such as the synthesizer frequency; reference-oscillator warping; adapt-timer duration; modulation-attenuator setting; and auxiliary-control outputs, which select one of four voltage-controlled oscillators, can be programmed through a serial peripheral interface (SPI). The SPI is connected to the controller microcomputer via three programming lines, namely the data (pin 7), clock (pin 8), and the chip enable (pin 9) of U6751 (Figure 3-42).

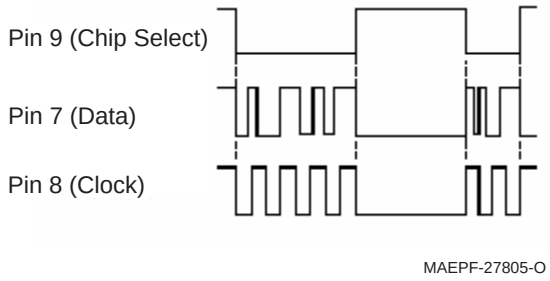

Figure 3-42. Waveform Representation During Programming of the LV Frac-N IC

3.7.4.3 Voltage Multiplier

Pin 12 (VMULT3) and pin 11 (VMULT4) of U6751, together with diode arrays D6751 and D6752 and their associated capacitors C6763, C6766, C6769 and C6771, form the voltage multiplier. The voltage multiplier generates 12.0 Vdc from the 3.0-V supply to supply the phase detector and charge-pump output stage at pin 47 (VCP) of U6751. This voltage multiplier is basically a stacked, multiple-diode capacitor network driven by two 1.05 MHz, 180 degrees out of phase signals from pins 12 and 11 of U6751.

3.7.4.4 Superfilter

The superfilter is an active filter that provides a low-noise supply for the VCOs, receiver and transmitter injection amplifiers. Regulator U0950, located in the controller section, supplies 9.3 Vdc to the FGU section thru the filtering network consisting of L6755, C6806, C6807, and C6818. This voltage is applied to pin 30 (SFIN) of U6751 and the emitter of Q6759. The output is a superfiltered 8.2 Vdc at the junction of pin 28 (SFOUT) of U6751 and the collector of Q6759. Filtering is accomplished with capacitors C6808, C6790, and C6791 at the output of this circuit and C6775 at pin 26 of U6751.

3.7.4.5 Modulation

To support many voice, data, and signaling protocols, XTL 5000 radios must modulate the transmitter carrier frequency over a wide audio-frequency range, from less than 10 Hz up to more than 6 kHz. The LV Frac-N IC supports audio frequencies down to zero Hz by using dual-port modulation. The audio signal at pin 10 (MODIN) is internally divided into high- and low-frequency components, which modulate both the synthesizer dividers and the external VCOs through signal MODOUT (pin 41). The IC is adjusted to achieve flat modulation frequency response during transmitter modulation balance calibration using a built-in modulation attenuator.

The Digital-to-Analog Converter (DAC) IC (U0900), and switched-capacitor filter (SCF) IC (FL0900) form the interface between the radio's DSP and the analog input of the LV Frac-N IC.

3.7.4.6 Charge Pump Bias

External circuitry connected to pin 39 (Bias 2) and pin 40 (Bias 1) of U6751 determine the current that is applied to the charge-pump circuitry. During receive mode, resistors R6768, R6769, and R6766 set the current supplied to pin 40 (Bias 1). Transistor Q6757 and resistors R6763, R6762, and capacitor C6795 form a circuit that momentarily increases the current to pin 40 (Bias 1) during receiver programming of U6751. This circuit is activated by pin 46 (ADAPTSW) of U6751 during the transition of programming U6751 to frequency and effectively decreases the length of time for the synthesizer to lock on frequency. Similarly, during transmitter mode, resistors R6768, R6769, and R6768 set the current supplied to pin 39 (Bias 2). Transistor Q6758 and resistors R6770, R6767, and capacitor C6794 form a circuit that momentarily increases the current to pin 39 (Bias 2) during transmitter programming of U6751.

3.7.4.7 Loop Filter

The loop filter operates in synchronization with the phase detector of U6751 in two modes, normal and adapt. In normal mode, the loop filter forms a third-order loop filter consisting of components R6764, R6765, R6761, C6776 to C6779, and C6785 to C6789.

Pin 43 (IOUT) of U6751 provides the charge-pump current for steering of the control voltage line to the VCOs. During normal mode, pin 45 (IADAPT) is set to a high impedance and has no effect on the loop filter. When U6751 is programmed to a new frequency, the IC is initially operated in adapt mode. In this mode the loop filter is reconfigured for a wider bandwidth allowing the synthesizer to lock faster. The charge-pump output is supplied through pin 45 (IADAPT) in this mode, and this reconfigures the loop filter to behave like a second-order filter.

3.7.4.8 Lock Detect

Lock status of the synthesizer loop is provided to the microprocessor by pin 4 (LOCK) of U6751. A high level (3.0 Vdc) indicates that the loop is stable. A low voltage indicates that the loop is not locked and will result in a Fail 001 to be displayed on the control head display.

3.7.4.9 Transmitter Injection

The transmit (TX) injection string consists of three amplifier stages (Q6764, Q6765, and Q6766) whose main purpose is to maintain a constant output to drive the RF power amplifier and supply the TX feedback signal to the FGU synthesizer loop. The first two stages are powered by the superfiltered 8.2 Vdc, which is decreased by 0.7 Vdc via the dual diode D6750, resulting in a 7.5 Vdc supply. The third stage is powered by the keyed 9.1 Vdc and the TX injection string is on only with keyed 9.1 Vdc activated during transmit mode. The TX VCO output is attenuated 3 dB via resistors R6829 through R6831. This output is coupled to the first-stage amplifier Q6764, further attenuated 3 dB via resistors R6809 through R6811, and then coupled to the second-stage amplifier Q6765. This output is tapped to supply the TX feedback signal to the synthesizer prescalar, and the balance is further attenuated 3 dB via resistors R6816 through R6818. This output is coupled to the third-stage amplifier Q6766, further attenuated 3 dB via resistors R6825 through R6827, and coupled to the input of the RF power amplifier section. The four sets of resistive attenuators provide increased isolation between the TX VCO and RF power amplifier.

3.7.4.10 Receiver Injection

The receiver (RX) injection string is a two-stage amplifier that supplies the RX feedback signal to the FGU synthesizer loop and supplies the first local oscillator (LO) signal to the RX front-end mixer. The RX VCO output is attenuated 6 dB via resistors R6793 through R6795 to increase isolation. This buffered signal is amplified by the first-stage amplifier Q6762, which is supplied by the 8.2-V superfilter for a gain of approximately 10 dB. Resistors R6789, R6790, and R6796 through R6798 bias Q6762 to approximately 5 V and 35 mA. L6757 serves as a choke inductor; C6819 and C821 are added for filtering. The output of Q6762 is split into two paths. The first path feeds back to the synthesizer prescaler through blocking capacitor C6822. The second path, which supplies the LO signal to the RX front-end mixer, is attenuated 3 dB via resistors R6799, R6800, and R6824 to increase isolation. This buffered signal is amplified by the second-stage amplifier Q6763, which is supplied by the 9.3-V regulator for a gain of approximately 15 dB. Resistor R6801 biases Q6763 to approximately 4.5 V (±1 V, due to possible part variations). L6758 serves as a choke inductor; C6823, C6824, and C6826 are added for filtering. The output of Q6763 is passed through blocking capacitor C6825 and attenuated 3 dB via resistors R6802 through R6804 to increase isolation and supply approximately 15.5 dBm to the LO port of the mixer.

3.7.4.11 Transmitter VCOs

Transmitter frequencies are generated from two VCOs contained in U6754. U6754 is not serviceable and should be replaced if it is determined to be non-functional. Transmitter frequencies in the range of 764 to 776 MHz (repeater talkaround) and 794 to <806 MHz (trunking or repeater mode) can be generated when Aux1 (pin 48) of U6751 is active high (3.0 Vdc). This 3.0 volts is applied to transistor switch Q6753 allowing the superfiltered 8.2 Vdc supply to be connected to pin 2 (SWBPOSC1), bias for the first VCO of U6754. Likewise, transmitter frequencies in the range of 806 to 825 MHz (trunking or repeater mode) and 851 to 870 MHz (repeater talkaround) can be generated when Aux2 (pin 1) of U6751 is active high (3.0 Vdc). This 3.0 volts is applied to transistor switch Q6755 allowing the superfiltered 8.2 Vdc supply to be connected to pin 17 (SWBPOSC2), bias for the second VCO of U6754. Pin 20 (RFOUT) of U6754 is common to both oscillators and couples the oscillator's output signal to the first stage of the transmitter injection string. Modulation and frequency steering is accomplished through pin 8 (Cont_V) of U6754.

3.7.4.12 Receiver VCOs

Receiver first local-oscillator frequencies are generated from two VCOs in U6755. U6755 is not serviceable and should be replaced if determined to be non-functional. For receiver frequencies in the range of 764 to 776 MHz, high-side, first local-oscillator injection of 837.35 to 849.35 MHz (Fc + 73.35 MHz) is generated when Aux3 (pin 2) of U6751 is active high (3.0 Vdc). This 3.0 volts is applied to transistor switch Q6756 allowing the superfiltered 8.2-V supply to be connected to pin 2 (SWBPOSC1), bias for the first VCO of U6755. For receiver frequencies in the range of 851 to 870 MHz, low-side, first LO injection of 777.65 to 796.65 MHz (Fc - 73.35 MHz) is generated when Aux4 (pin 3) of U6751 is active high (3.0 Vdc). This 3.0 volts is applied to transistor switch Q6760 allowing the superfiltered 8.2-V supply to be connected to pin 17 (SWBPOSC2), bias of the second VCO of U6755. Pin 20 (RFOUT) of U6755 is common to both oscillators and couples the oscillator's output signal to the first stage of the receiver injection string. Frequency steering is accomplished through pin 8 (CONT_V) of U6755.

3.7.4.13 Prescaler Feedback

RF feedback for the synthesizer loop is provided by prescaler amplifier Q6761. Feedback from both the transmitter and receiver injection strings are coupled to this amplifier through resistor networks that both balance and attenuate the levels prior to amplification by Q6761. The output of Q6761 is coupled to U6751 at pin 32 (PREIN), which is the prescaler input for the synthesizer.

3.8 Controller Section

The controller section consists of a daughtercard module and associated circuitry to which it interfaces. It is the central interface between the various subsystems of the radio. Its main task is to interpret user input, provide user feedback, and schedule events in the radio operation, which include programming ICs, performing digital signal processing (DSP) on baseband audio and data, and sending messages to the control head display. Figure 3-43 on page 3-63 illustrates the components of the controller section.

The DSP section of the microprocessor performs digital vocoder (voice coder-decoder) functions previously performed by analog circuitry. This includes all tone signaling, trunking signaling, and conventional analog voice processing.

All analog signal processing is accomplished digitally using the Patriot IC microprocessor (U100). This microprocessor consists of a microcontroller, as well as a DSP. In addition, it provides a digital voice plus data capability utilizing IMBE voice-compression algorithms. *Vocoder* is the general term used to refer to these DSP-based systems.

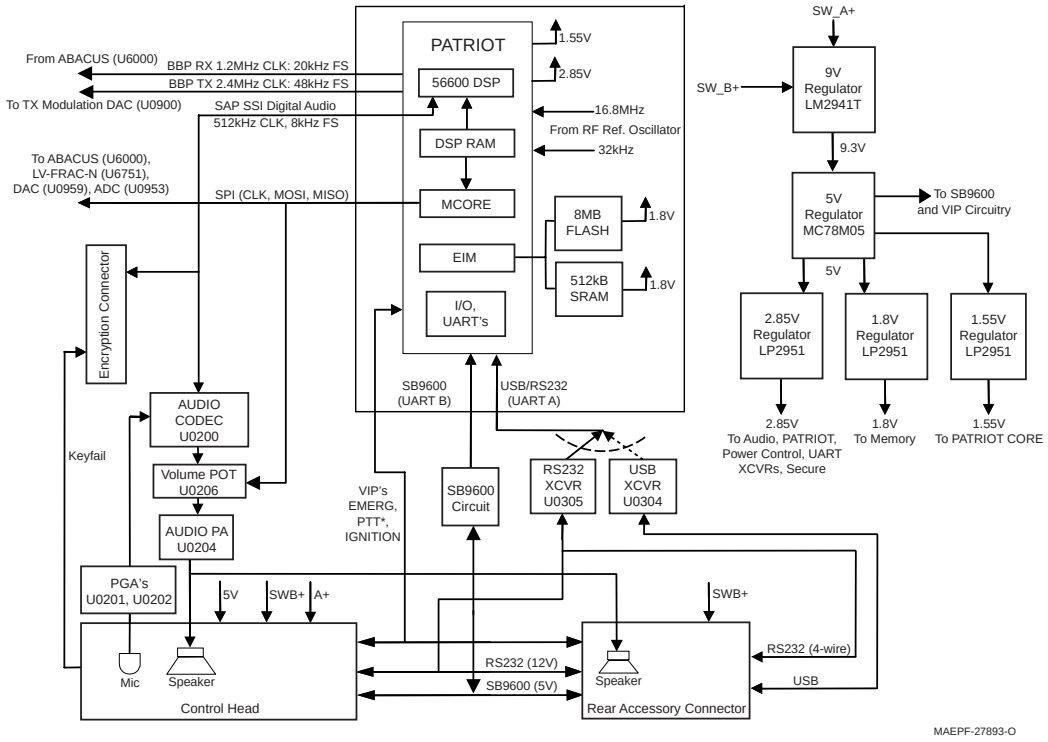

Figure 3-43. XTL 5000 Controller Section

The controller consists of digital logic comprised of a microprocessor (the Patriot IC, U100) and memory consisting of a 512K x 16 SRAM (U103) and a 4M x 16 FLASH ROM (U102). The microprocessor is a dual-core processor that contains a DSP56600 core and an MCORE microcontroller with custom peripherals. The term, *MCU*, refers to the MCORE controller section of the Patriot IC. The FLASH ROM contains the programs that the Patriot microprocessor executes and is used to store customer-specific information and radio-personality features that, together, constitute the *codeplug*. It allows the controller firmware to be reprogrammed for future software upgrades or feature enhancements. The SRAM is used for scratchpad memory during program execution.

The controller performs the programming of all peripheral ICs. This is done via a serial peripheral interface (SPI) bus and through General-Purpose Input/Outputs (GPIO) from the Patriot IC. ICs programmed through this interface include the LV Frac-N synthesizer, ABACUS III IC, D/A converter (DAC), A/-D converter (ADC), and volume digital potentiometer.

In addition to the SPI bus, the controller also maintains two asynchronous serial busses: the SB9600 bus and an RS-232/USB serial bus. The SB9600 bus interfaces the controller section to different hardware accessories, some of which may be external to the radio, including the control head. The RS-232/USB bus is used as a common data interface for external devices and for programming/ flashing the radio.

User input is from the control head and is sent to the controller through the SB9600 bus. Feedback to the user is provided by the control-head display.

The controller schedules the activities of the DSP, including setting operational modes and parameters. The DSP section of the processor contains an 84K x 24 program RAM, 2K x 24 program ROM, and 62K x 16 data RAM, which are all integrated into the Patriot IC. The vocoder subsystem consists of this DSP core, the modulation DAC (U0900), and the voice CODEC (U0200).

In receive mode, the ABACUS III IC provides data samples directly to the DSP for processing. In transmit mode, the DAC provides a serial D/A converter. The data generated by the DSP is filtered and reconstructed as an analog signal to present a modulation signal to the VCO (voltage-controlled oscillator) at the LV Frac-N synthesizer. Both the transmit and receive digital data paths between the DSP and the CODEC are through the Patriot IC BBP (Baseband Interface Port) SSI port.

The CODEC provides A/D conversion of the analog microphone signal and D/A conversion of the analog speaker output. During transmit, the microphone audio is passed through the gain/filtering analog circuitry to the CODEC, which translates the analog waveform to serial SSI data. This data is made available to the DSP through the Serial Audio Port (SAP) of the Patriot IC. Conversely, the DSP writes speaker data samples to the D/A in the CODEC through the SAP port. The CODEC provides an analog speaker output audio signal to the audio power amplifier, U0204.

3.8.1 Daughtercard Module

The daughtercard module (Figure 3-44) contains the central processing unit (CPU) of the radio. This module interfaces with other parts of the main board. This module primarily contains three sections:

- Microprocessor (Patriot IC: U100): consists of a controller and a DSP whose functions are described above in “3.8. Controller Section” on page 3-62.
- FLASH IC (U102): the firmware storage IC
- SRAM IC (U103): used by the microprocessor to perform its memory operations

NOTE: The three sections of the daughtercard module are highly susceptible to ESD and moisture damage. Extreme care is advised when handling or servicing the main board.

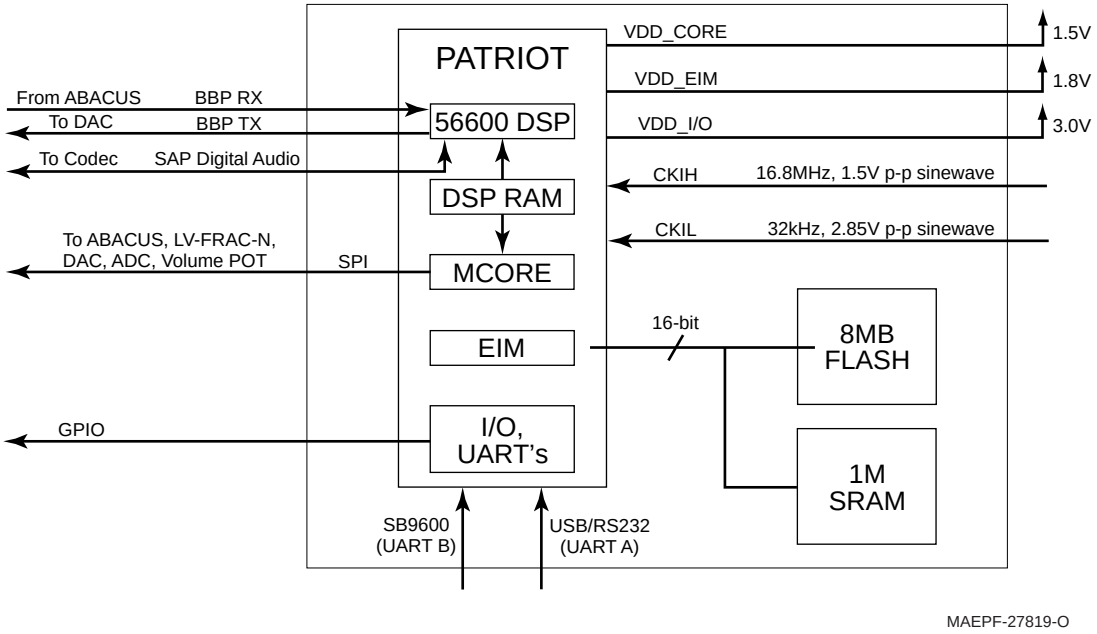

Figure 3-44. XTL 5000 Daughtercard Module

3.8.2 Controller DC Power Distribution

Figure 3-45 illustrates the controller DC power distribution circuitry.

The A+ power for the radio is derived from the 12-V battery, which is applied to the main board through connector J0950. This A+ voltage is routed to the control-head connector, J0401, pins 19 and 21, to the control head.

A power FET (Q51) provides the means of controlling the main power source (SWB+) by the on/off switch. SWB+ is routed back to the main board through connector J0401-17 and out the rear connector, J2-24.

SW_B+ turns on controller FET switch Q0503, which supplies SW_A+ to regulator U0500. This 9.3-V regulator powers up the main 5-V controller regulator U0503. The 5-V supply powers on all four controller regulators:

- U0962 (3.0 V) for the power control section
- U0503 (2.85 V) for the controller and daughtercard I/O
- U0507 (1.85 V) for the memory
- U0502 (1.55 V) for the microprocessor core.

The SW+5-V regulator is the main power source for the controller.

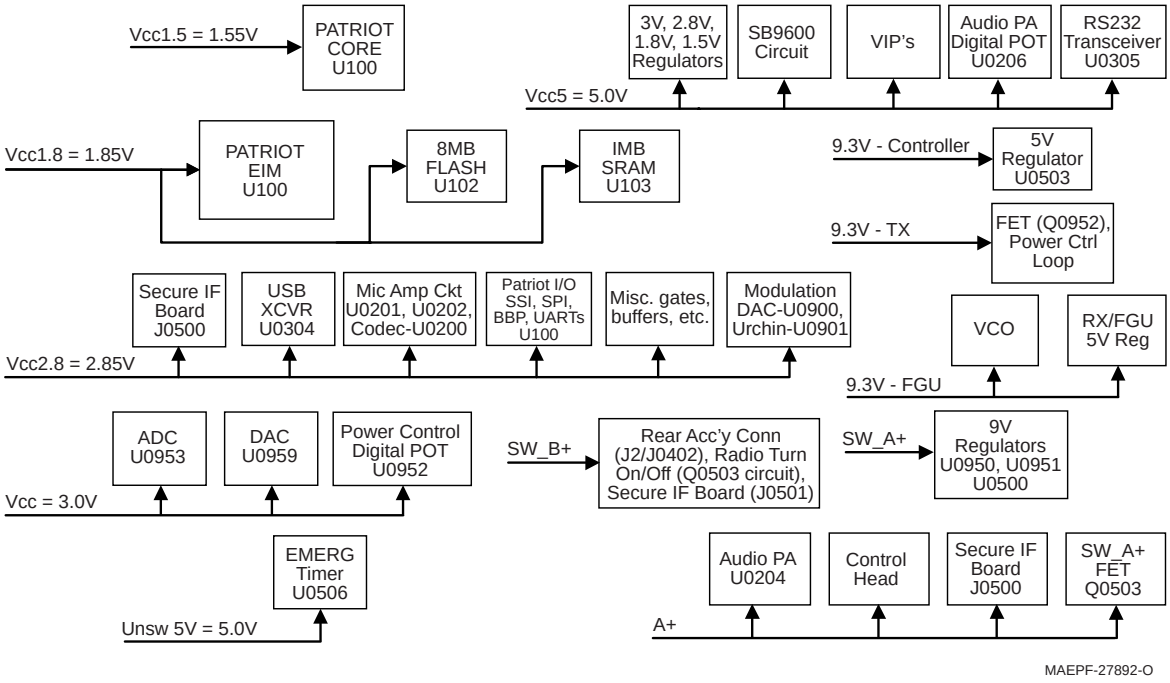

Figure 3-45. B+ Routing for Controller Section

On the secure interface board, U800, Q802, and Q803 provide SWB+ to the encryption module (if equipped). The SWB+ and UNSWB+ encryption voltages both originate from the secure interface board and are fed to the encryption module via J0701 and J0501.

It should also be noted that a system reset is provided by the undervoltage detector, U0504. This device brings the system out of reset on power-up, and provides a system reset to the microcomputer on power-down.

The various voltages used by the ICs on the main board are shown in Table 3-13.

Table 3-13. Integrated Circuits Voltages

Integrated Circuit	UNSW5V	SW 5V	A+	3.0 V	2.85 V	9.3 V_TX	1.85 V	1.55 V
Patriot Microprocessor					U100		U100	U100
Flash							U102	
SRAM							U103	
A/D				U0953-28				
D/A				U0959-4				
Modulation D/A					U0900-3 FL0900-4			
Urchin					U0901			
RS-232 XCVR		U0305-16						
USB XCVR					U0304-7			
Audio PA			U0204-7					
CODEC					U200-6			
Amplifiers, EPOTs					U0201-4 U0202-3			
555 Timer	U0506-4							
SB9600 MUX		U606-16						
Volume Pot		U0206-7						
32K Crystal					Y0100-5			
Modulation MUX					U0902-16			
Power Control						U0956-4 U0957-4 U0960-4		
Keyed 9.1 V Switch						Q0952		

3.8.3 Encryption Voltages

The secure interface board produces two voltages sourced by A+ and SW_B+ through J0501, pins 10 and 9, that are used by the encryption module: UNSW_B+_ENC (7 V) and SW_B+_ENC (7 V). The constant 7 V is generated using U800, Q802, and Q803 and is fed to J0701. At the secure interface board, the 7 V provides continuous unswitched voltage when the vehicular battery is connected to the radio and is also switched to provide SWB+ to the encryption module. A 5-V storage circuit, C810 (0.47-farad capacitor), provides +5 Vdc to the encryption module via J0701, pin 12, to hold encryption keys for a period of three days with no A+ voltage present. The 5 V and 2.85 V controller supplies are used to provide logic translation between the legacy keyloader data (5 V) and the universal crypto module (UCM) (3 V). The secure interface board also supplies the UCM chip-select logic line and the other control lines, clocks, and other components, to the main board microprocessor.

3.8.4 Reset Circuits

The reset circuits consist of the power-on reset (POR*) circuit (Figure 3-46), SW_B+ sense circuit, and SB9600 bus reset circuit. These circuits allow the microprocessor to recover from an unstable condition, such as removing battery A+ from the radio while it is on, battery voltage too low, and miscommunication to remote devices on the SB9600 bus, as well as generally monitoring the power on/off condition.

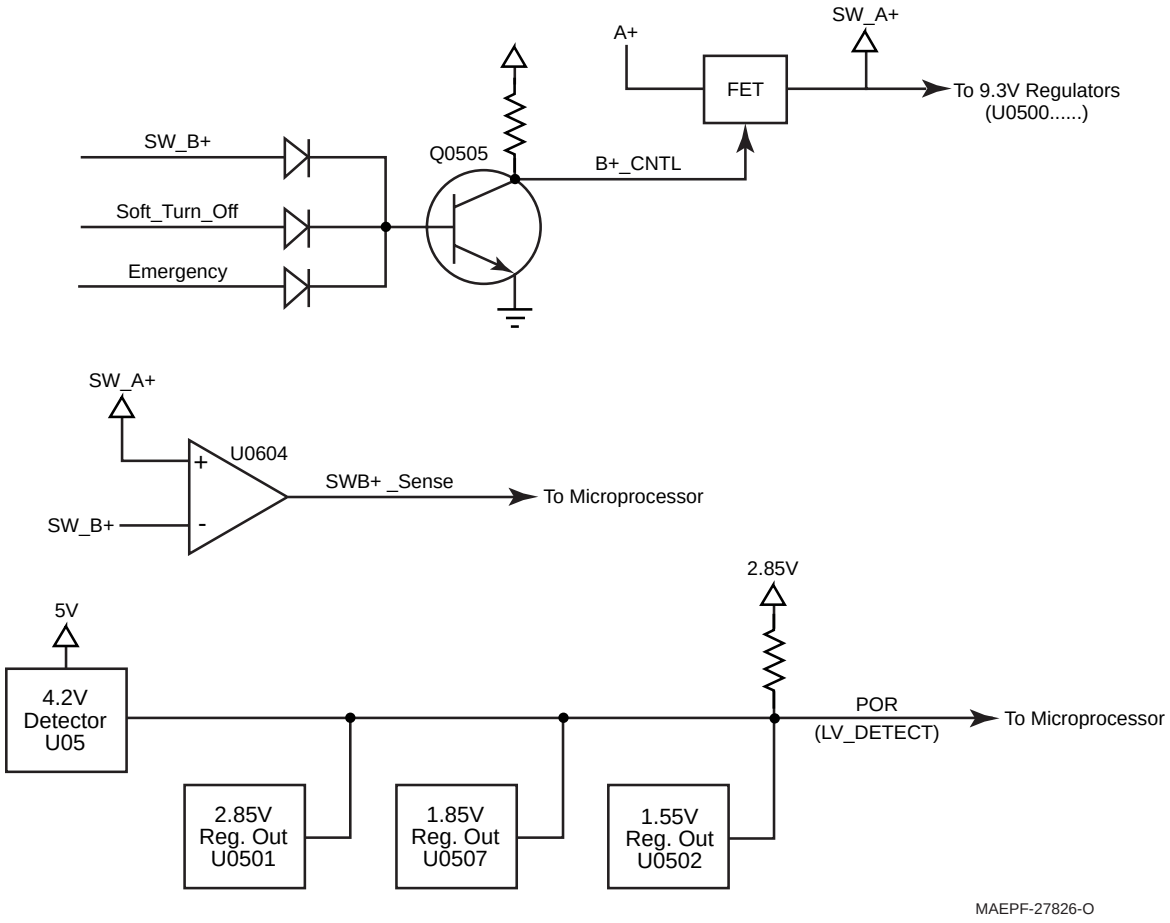

Figure 3-46. Power-On Reset Circuit

The SW_B+ and A+ voltage levels are sensed by the comparator circuit consisting of U0604, Q0505, and R0505, R0506, R0508, and R0509. When SW_B+ goes below 8.5 V or SW_A+ goes below 10 V, U0604-7, SW B+ Sense, goes low. When this occurs, the radio completes its soft power-down and eventually drives the Soft_Turn_Off line low, which turns off Q0502 and FET Q0503. This turns off SW_A+ and eventually turns off the 9-V, 5-V, 3-V, 2.85-V, 1.85-V, and 1.55-V regulators.

The POR* circuit consists of a wired-OR circuit of the error output lines from the 2.85-V, 1.85-V, and 1.55-V regulators, which indicates a failure of either of these regulators; and a reset output from a 4.2-V detector IC U0504. When either of the regulators fails or the 5-V supply begins to drop below 4.2 V, POR* is asserted low, resetting the microprocessor U100 at U001, LV_DETECT.

When the radio is operating correctly (A+ > 10 V and SW_B+ > 8.5 V), SW_A+ and VOCON regulators U0501, U0502, and U05007 are at normal voltage. The POR* line and SW_B+_Sense are high (2.85 V).

The other signal that can cause a processor/radio reset is the SB9600 RESET line. The RESET line is driven high (5 V) by a remote device that is having problems communicating with the processor.

3.8.5 Power-Up/Power-Down Sequence

The XTL 5000 radio power is cycled via SW_B+ (battery voltage level). This voltage is supplied by the control head via J0401, pin 17, when the On/Off button is cycled.SW_B+ is derived from the battery A+ voltage via a power FET in the control head (W5 and W7 models).

3.8.5.1 Power Turn-On

When SW_B+ is active at turn-on time, the voltage turns on Q0501, Q0504, and Q0505, which then turns on SW_A+ via the power FET Q0503. SW_A+ then supplies all radio power (9.3-V regulators and controller regulators). SW_A+ is derived the same way SW_B+ is at the control head.

SW_B+ is also sent to the comparator circuit, U0604, which allows the processor to monitor its level via SW_B+_Sense (active high). When SW_B+ is sensed “on” by the processor, it asserts high an output line, Soft_Turn_Off, to the wired-OR turn-on circuit at Q0502. This active-high processor output is required for performing a soft power-down.

3.8.5.2 Power Turn-Off

At turn-off, SW_B+ becomes inactive at the control heads. As this voltage falls below 8.5 V, the U0604 comparator circuit drives SW_B+_Sense low, telling the processor to power down the radio. The processor eventually de-asserts low the SOFT_TURN_OFF signal after keeping the wired-OR turn-on circuit, and thus SW_A+ and all radio power, on long enough to perform a soft power-down, which includes deaffiliating on a trunked system, saving radio status parameters, etc. Once the SW_B+ and SOFT_TURN_ON lines are both low, Q0502 and Q0504 turn off, which provides a low at power FET Q0503. This turns off SW_A+, which removes all radio power.

3.8.5.3 Emergency Power-Up/-Down Sequence

The emergency input is provided to enable the radio transceiver to be activated, regardless of the state of the control head’s On/Off switch. The emergency input is activated by opening the normally grounded footswitch connected to either J0401, pin 18, or J0402, pin 28, of the controller. This input is routed to Q0501 and to the same wired or turn-on circuit and SW_A+ FET.

Under normal configurations, the output of Q0501 goes low to trigger pin 2 of a monostable vibrator U0506 causing the output pin 3 to go high. This enables the regulators through D0501 and Q0502. It also enables the EMERG_SENSE line to the MCU through U0508-1. The monostable vibrator is a timeout timer that holds the regulators on for 300 ms. This delay is required to allow the MCU to initiate its start-up vectors and poll the EMEG_SENSE line J17 of U0001. The MCU takes control of the regulators through D0501 and Q0502 by holding SOFT_TURN_OFF high.

The emergency active state depends on the emergency polarity into the timer. Normally with Q0501 present, emergency is active with the footswitch open. Removing Q0501 and adding R0527 causes the emergency to go active with the switch closed.

3.8.6 MCU and DSP System Clocks

The MCU within the Patriot IC (U100) needs two clocks for proper operation. A 16.8 MHz sine-wave reference is provided at the CKIH (A6) pin of the Patriot IC. The source of this clock is a 16.8 MHz oscillator and its associated filtering circuitry. This clock is also provided to the Urchin IC (U0901). The MCU has the capability of running at higher clock rates, which are programmable and based on this 16.8 MHz reference. The DSP within the Patriot IC also uses the 16.8 MHz provided at the CKIH (A6) pin as a reference.

The Patriot IC also requires a 32 kHz square-wave clock, provided at the CKIL (J7) pin. This clock is generated by a 32 kHz crystal (Y0100), with supporting circuitry for oscillation. This clock is utilized only for the Patriot IC, and is used for reset capability and other Patriot IC functions.

Four additional clocks are also supplied to the daughtercard: a 20 kHz RX frame-sync clock, a 48 kHz TX frame-sync clock, a 1.2 MHz RX data clock, and a 2.4 MHz TX data clock. The microprocessor also generates the digital audio bus clocks: a 512 kHz data clock and an 8 kHz frame-sync clock.

3.8.7 RS-232 USB Bus

The XTL 5000 microcontroller in the Patriot IC (U100) has two internal UARTS that can be configured for RS-232 data communication: UARTA and UARTB (Figure 3-47).

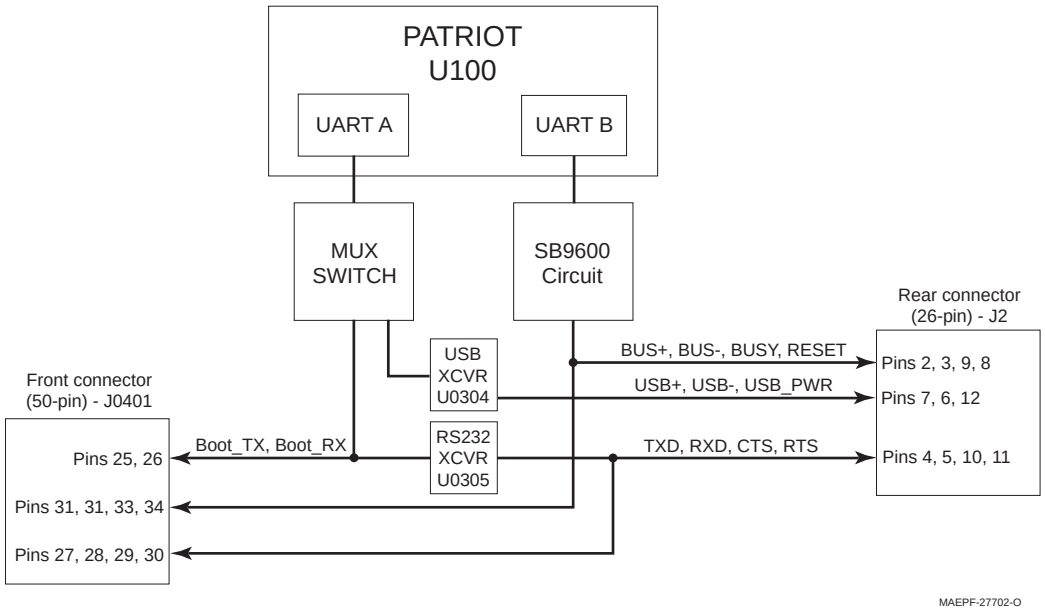

Figure 3-47. Patriot IC (U100) UART Configuration

UARTA is configured for RS-232 data transmission by default, and its data transmission is routed through an on-board RS-232 transceiver (U0305) to bring the data voltage levels up to EIA RS-232 standards before the data exits the front and rear of the radio. The U0305 is a two-driver, two-receiver device, protected against ±15 kV electrostatic discharges.

For data output, UARTA transmits data from the microcontroller at 0-V and 2.85-V levels. This data is sent on an asynchronous serial bus, which is routed to an on-board RS-232 transceiver (U0305) that converts these low-voltage levels to -9 V and +9 V signal levels. This RS-232-formatted data is routed out the front of the radio (J0401-27, J0401-28, J0401-29, J0401-30) and to the rear of the radio (J0402-7, J0402-8, J0402-9, J0402-10).

For data input, U0305 can accept up to ±30-V signal levels. These high levels are converted inside the U0305 down to 0-V and 5-V levels. Next these data levels are routed thru a buffer stage (U0303) which lowers the data to 0-V and 2.85-V levels. This is the required voltage levels for the input into the microcontroller.

This radio meets EIA compatibility with external data accessory devices. The naming scheme (see Table 3-14 and Table 3-15) used for the microcontroller's RS-232 lines sometimes conflict with EIA RS-232 naming schemes. This is due to the microcontroller's pin names versus I/O direction, compared to the EIA pin names versus I/O direction. Therefore, a matching naming scheme has been developed. If the pin is coming from the UART, the pin name has UART in the name. However, if you want to know how the EIA standard identifies the pin, a chart exists that provides the naming conversion. The shipping rear data cable automatically routes the pins according to the EIA standard, so interfacing to external data devices, such as computers, is done correctly. The naming scheme information is only needed when the rear connector is opened and the wires need to be identified for connection to a custom device. Note that the correct interfacing of RS-232 lines is "output line" to "input line". For example, the TX pin of one device connects to the RX pin of the other device, and the RTS pin of one device connects to the CTS pin of the other device. Never connect TX to TX, RX to RX, and so on.

Table 3-14. Rear Connector Naming Scheme

Radio Pin Direction	J2 Pin No.	J2 Pin Name	Pin Alternate Name	EIA-Compatible Name at Rear Conn. J2	P2 Rear Accessory Cable DB9 (Female) = DCE Interface		DB9 (Male) Serial Port Connector = DTE Interface	Data Device Pin Direction
Output	4	UARTA_TX	No Change	TX_DCE	TX_DCE = pin 2	<-->	pin 2 = RX_DTE	Input
Input	5	UARTA_RX	No Change	RX_DCE	RX_DCE = pin 3	<-->	pin 3 = TX_DTE	Output
Output	10	UARTA_CTS	Becomes RTS	RTS_DCE	RTS_DCE = pin 8	<-->	pin 8 = CTS_DTE	Input
Input	11	UARTA_RTS	Becomes CTS	CTS_DCE	CTS_DCE = pin 7	<-->	pin 7 = RTS_DTE	Output

Note: Connecting to a computer = DTE device
TX to RX and RTS to CTS

Table 3-15. Remote-Mount Interconnect Board Connector Naming Scheme

Radio Pin Direc-tion	J6 Pin No.	J2 Pin Name	Pin Alternate Name	EIA-Compatible Name at Rear Conn. J2	P2 Rear Accessory Cable DB9 (Female) = DCE Interface	HKN6122 Data Cable DB9 (Female) = DCE Interface		DB9 (Male) Serial Port Connector = DTE Interface	Data Device Pin Direc-tion
Output	2	RS232_RXD	Becomes TX	TX_DCE	pin 2 = TX_DCE	TX_DCE = pin 2	<-->	pin 2 = RX_DTE	Input
Input	3	RS232_TXD	Becomes RX	RX_DCE	pin 3 = RX_DCE	RX_DCE = pin 3	<-->	pin 3 = TX_DTE	Output
Output	17	RS232_CTS	Becomes RTS	RTS_DCE	pin 17 = RTS_DCE	RTS_DCE = pin 8	<-->	pin 8 = CTS_DTE	Input
Input	4	RS232_RTS	Becomes CTS	CTS_DCE	pin 4 = CTS_DCE	CTS_DCE = pin 7	<-->	pin 7 = RTS_DTE	Output

Note: Connecting to a computer = DTE device
TX to RX and RTS to CTS

3.8.8 Serial Communications on the External Bus (SB9600)

The SB9600 bus is an asynchronous serial communication bus using a Motorola-proprietary protocol. It provides a means for the microcontroller within the Patriot IC (U100) to communicate with other hardware devices. In the radio, it communicates with hardware accessories connected to the accessory connector and the remote interface board. Serial communications on this external bus uses three of the four SB9600 lines: BUS+ (J0401-31), BUS- (J0401-32), and BUSY (J0401-33) data lines originating from the microcontroller's secondary UART.

These three lines are bidirectional; therefore, numerous devices can be in parallel on the bus. All devices monitor the bus while data is being transmitted at a 9600-baud rate. The transmitted data includes the address of the device for which the data is intended. Examples of the different types of data are: Button press/release data, sent to and from the radio's microprocessor; control-head display data; and the existence of accessories on the bus, such as Siren or VRS. The use of these accessories requires the existence of SB9600 protocol on one of the radio's data buses.

The microcontroller sends the data transmission from UARTB, onto the bus at 0-V and 2.85-V levels. Next, the software sets microcontroller SB96_RS232_EN to a logic HIGH. Buffers (U0602 and U0603) are now powered and the data is changed to the SB9600 format via pull-up and pull-down logic circuitry. SB96_RS232_EN also sets the data MUX (U0606) to route the new SB9600-formatted data to the correct lines at the front of the radio (J0401-31, J0401-32, J0401-33, and J0401-34) and to the rear of the radio (J0402-3, J0402-4, J0402-5, and J0402-6). Since SB96_RS232_EN is kept HIGH as the default state, the UARTB default function is for SB9600 data traffic only. This is true for the radio in either dash- or remote-mount configuration.

When the microcontroller sends data onto the bus, the microcontroller monitors the transmitted data as a collision-detection measure. If a collision is detected as a result of receiving a different data pattern, the microcontroller will stop transmission and try again; that is, when the RESET line (J0401-34) is used.

Data bus drivers for the BUS+ and BUS- lines are differentially driven, having BUS- inverted from the state of BUS+. The drivers are so designed that any of the devices on the bus can drive these lines to their non-idle state without loading problems.

In a typical data transmission, the microcontroller examines the BUSY line. If the BUSY line is in the idle state, the microcontroller sets the BUSY line HIGH, and then it transmits using BUS+ and BUS-. At the end of the transmission, the microcontroller returns the BUSY line to idle.

The idle states for the SB9600 lines are: BUS+ = logic HIGH, BUS- = logic LOW, BUSY = logic LOW, and RESET = logic LOW.

3.8.9 Serial Peripheral Interface (SPI) Bus

The microcontroller (U100) utilizes an SPI bus for configuring and operating specific ICs in the controller and RF sections of the radio. The SPI bus is a synchronous serial bus made up of four lines (see Figure 3-48 on page 3-72). The CLK line is used to control the speed of the data to/from the IC and the microcontroller. If necessary, this clock speed can be adjusted to a different value for each IC.

The Data-OUT pin receives a data string from the microcontroller. The Data-IN pin sends a serial data string to the microcontroller, usually to indicate what the current programmed values are of the IC. The Chip Select pin is used to select which single IC is currently being programmed. Each ICs Chip Select pin is hardwired to a specific SPI bus and can only be controlled by that bus. The microcontroller pulls the ICs chip-select line LOW to enable the IC for receiving configuration data, for programming, or for sending out its existing configuration state. Additional SPI buses allow chip selecting to occur in parallel. Therefore, the operations on each SPI bus do not add any delay to the activities occurring on another SPI bus.

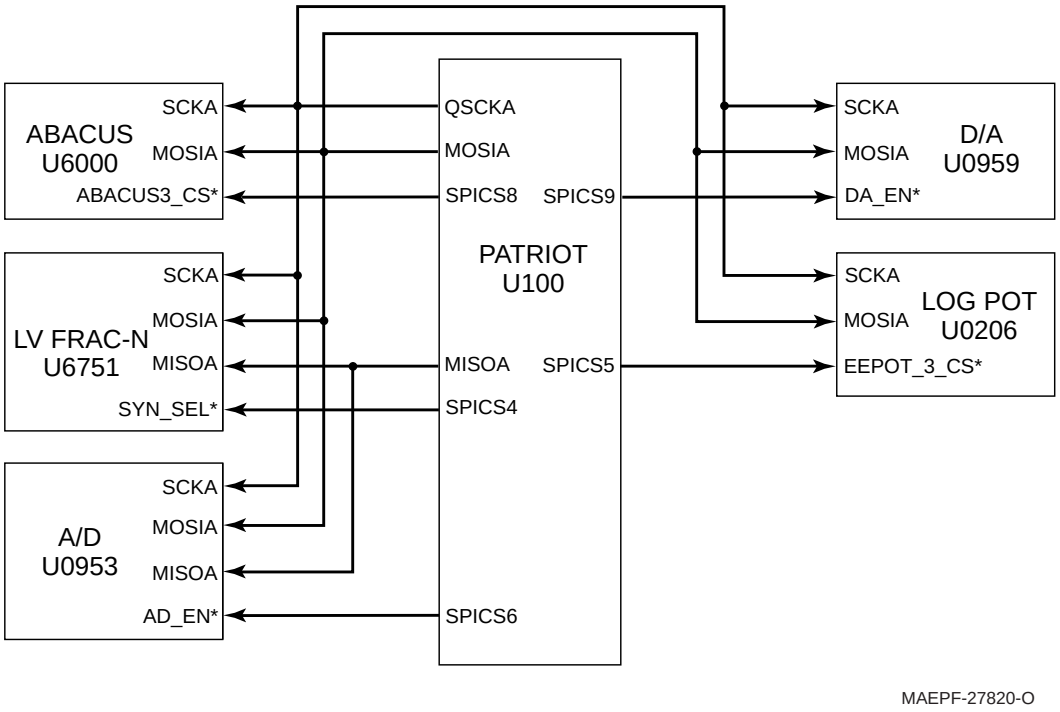

Figure 3-48. Serial Peripheral Interface (SPI) Block Diagram

The following ICs are controlled and programmed by SPI_A:

- ABACUS III (U6000): Sigma Delta A/D converter and 2nd LO frequency adjust. The ABACUS III IC has a single pin for both input and output. Therefore, additional circuitry (U0103 and U0105) handles the SPI_MISO or the SPI_MOSI data lines from the microcontroller and allows a read or write operation to occur with the ABACUS III IC via a single bidirectional data line.
- A/D (U0953): monitors temperature, source voltage, PA current, feedback-voltage loop, forward-detected voltage, and reverse-detected voltage
- D/A (U0959) (microcontroller only writes to IC): controls bias stages 1-4, sets current limit, monitor thermistors, tuner overall RF power, and adjusts RX filter
- LV Frac-N (U6751) (microcontroller only writes to IC): scales the frequency from the VCO, control RX, and TX feedback loops
- EPOT (U0206) (microcontroller only writes to IC): controls the 32 steps of audio volume (vol=0: low to 15: high) that is routed to audio PA

3.8.10 Receive Audio

The controller processes all received signals digitally. This requires a unique back-end from a standard analog radio. This unique functionality is provided by the ABACUS III IC as the interface to the DSP. The ABACUS III IC (in the receive back-end section of the transceiver) provides a digital back-end for the receiver. It provides digital output data words at a 20 kHz sampling rate (refer to section “3.5. Receiver Back-End” for more details on ABACUS III IC operation). This data is passed to the DSP through the RX Baseband Interface Port (BBP). The SPI bus is used to configure the operation of the ABACUS III IC and is driven by the Patriot IC. ABACUS_DIN is the data line on which the RX data words are transferred from ABACUS III IC to the Patriot IC (refer to Figure 3-49 on page 3-73).

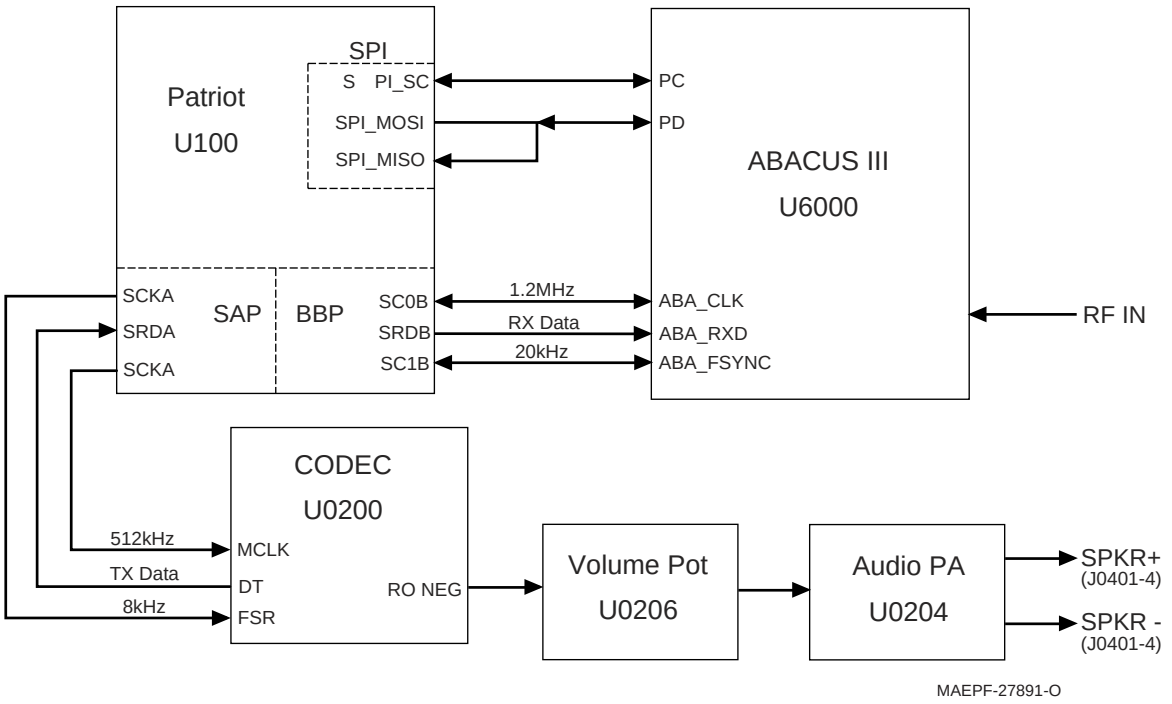

Figure 3-49. XTL 5000 RX Signal Path

The ABACUS III data is transferred to the Patriot IC at a 1.2 MHz bit rate, which is a synchronous clock provided by the ABACUS III IC. The 20 kHz interrupt clock, also provided by the ABACUS III IC, signals the arrival of a data packet and represents the sampling rate of the received data.

The DSP then processes this data to extract audio and signaling, perform filtering, alert-tone generation, etc. The DSP performs de-emphasis and discrimination before sending the discriminator data to the audio CODEC (U0200) via the SAP SSI bus. This bus is the digital audio bus consisting of the 512 kHz master bit clock (SAP_DCLK), and the 8 kHz frame sync (SAP_FSYNC). These clocks represent the data bit rate and sampling rate, respectively, for both the transmit and receive digital audio. For secure messages, the digital signal data must be passed to the secure module for decryption prior to DSP processing of the speaker data. The DSP transfers the data to and from the secure module through the SAP SSI port TXD and RXD signals. Configuration and mode control of the secure module is performed by the MCU through this bus.

The CODEC D/A analog output signal is routed to the RX_FILT_AUDIO line at both J0401 and J0402/J2 for legacy accessories and special applications products at an amplitude of 100 mV per kHz of deviation. The signal amplitude is independent of volume setting. This output is also routed to a multiplex switch, U0210, which is one source of audio to the audio PA speaker output. The alternate PA source, AUX_RX, is an input from J0401 and is used with vehicular repeater systems (VRS). The multiplexer output, normally received speaker audio, is routed to a volume control digital programmable potentiometer, U0206, and then to the audio PA (U0204) input. The audio PA output then drives the external speaker.

The audio power amplifier (U0204), is a DC-coupled-output, bridge-type amplifier. The gain is internally fixed at 40 dB. Speaker audio leaves U0204 on pins 4 and 6. For dash-mount radios, the audio is routed to the speaker via J0402, pins 19, 21, 23, and 25, and then to J2, pins 20 and 26. The amplifier is biased to one-half of the A+ voltage. An audio isolation transformer must be used if grounded test equipment, such as an audio analyzer or service monitor, is to be connected to the speaker outputs.

Caution

The speaker outputs must NOT be grounded in any way.

Normally, R0220 pulls up U0204, pin 8, to SW_B+ to enable the audio PA. When the radio is squelched, the audio PA is muted by the microprocessor. Q0200 is enabled to provide approximately 4.5 V through a voltage divider (Q0200 and R0222) to U0204, pin 8, which mutes the audio PA. When SW_B+ is turned off, the voltage from SW_A+ on U0204 falls below 2 V, placing the audio PA in standby, which turns off the U0204 output transistors to the speaker. Table 3-16 shows the voltages present at U0204, pin 8, during its various conditions.

Table 3-16. PA Condition Voltages at U0204, Pin 8

Power Amplifier Condition	U0204 Pin 8 (Vdc)
Standby	0-2
Mute	3.3-6.4
Enabled	8.5-17

3.8.11 Transmit Audio

The mobile microphone connects to the front of the control head through connector P104. Microphone audio (MIC_HI) enters the main board via J0401, pin 4, and is routed to multiplexer U0209 (refer to Figure 3-50 on page 3-75). Resistors R0200 and R0204 provide 9.6 Vdc bias voltage for the microphone's internal circuitry.

The multiplexer allows TX modulation audio to be routed from one of 3 possible sources: mobile microphone (MIC_HI), AUX_MIC (audio sourced from the J2 rear accessory connector in motorcycle configuration), or AUX_TX (audio from a VRS). The resulting audio source is then sent to a two-stage, programmable gain/attenuation circuit comprised of U0201 and U0202. The gain is accomplished via a programmable digital potentiometer in the amplifier circuit. This gain is adjustable via CPS and is programmed in ±3 dB steps. After passing through an anti-aliasing filter, audio is sent to the input of the CODEC (U0200) where it is digitized via its internal A/D converter. The digital audio data is then sent via the SAP SSI bus to the DSP at the Patriot IC. As with speaker data samples, the DSP reads the microphone audio samples and processes, pre-emphasizes, filters, and adds signaling information to this data. As with the received trunking data, low-speed transmit data is processed by the MCU and returned to the DSP. For secure messages, the digital signal data can be passed to the secure module prior to DSP processing and modulation. The DSP transfers the data to and from the secure module through the SAP SSI transmit (TXD) and receive (RXD) lines.

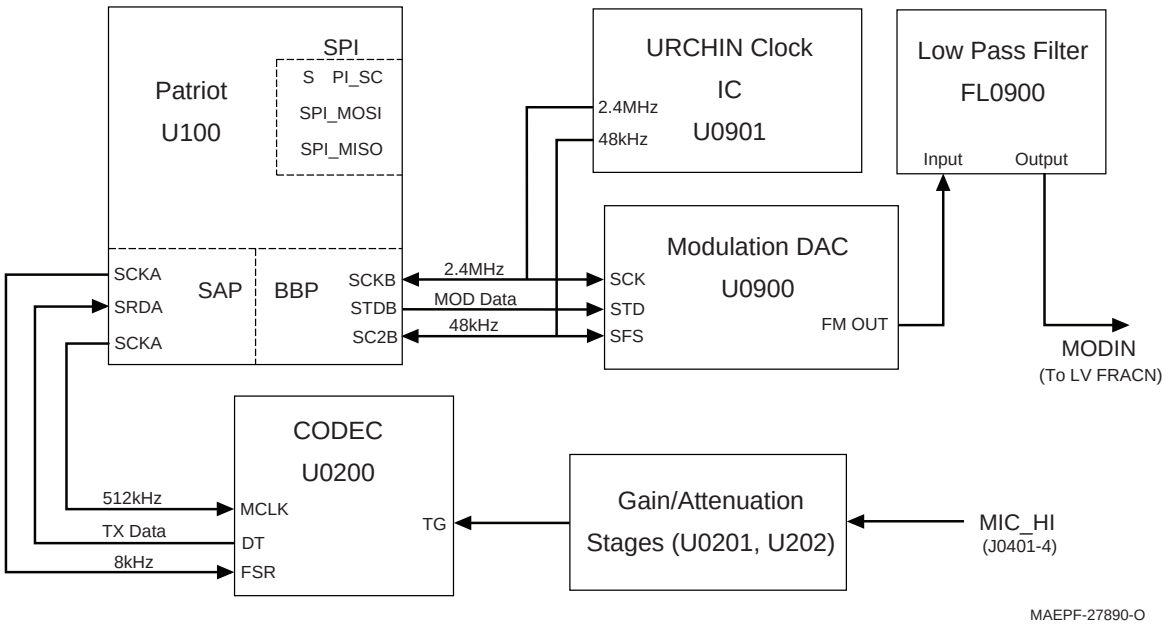

Figure 3-50. XTL 5000 TX Signal Path

After the DSP has finished its processing, filtering, and signaling on the audio data samples, it then sends this data to the modulation DAC (U0900) on the BBP SSI port, where it is converted to the analog modulation signal. The data is clocked over to the modulation DAC at a 2.4 MHz bit rate, with a frame sync (representing the transmit data sample rate) of 48 kHz. Both of these clocks are generated by the Urchin IC (U0901).

The modulation DAC audio output signal is sent to a switched capacitor low-pass filter (FL0900) that performs anti-aliasing filtering. The filter output is sent through a multiplexer switch, U0902, and finally on to the FGU/LV Frac-N synthesizer for modulation of the RF carrier signal.

3.8.12 Flash Programming

When the radio needs new program code, this can often be done by reflashing the FLASH ROM (U102) located on the daughtercard. Reflashing is accomplished by using a programming cable (HKN6155 for Mid Power or HKN6183 for High Power) and the Motorola Customer Programming Software (CPS) FLASHport tool. The technique to flash the radio is the same as when using CPS or the TUNER software to change features on your radio. Two data lines are utilized on the programming cable to allow the computer to communicate with the microcontroller. These two lines are called BOOT TX (J0401-25), and BOOT RX (J0401-26) (see Figure 3-51).

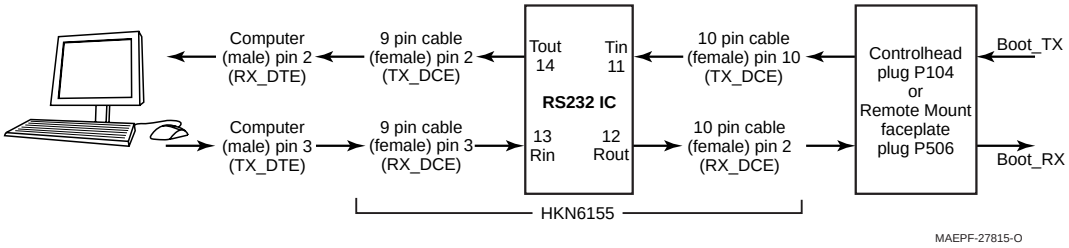

Figure 3-51. Boot RX and Boot TX Data Lines

The standard method of upgrading a radio's software and communicating between a computer and the radio microcontroller involves the use of the UART path via the programming cable. The radio is placed in a bootstrap mode whenever the programming cable is inserted into either the control- head microphone connector (P104) or the remote-mount interconnect board data connector (P506). This cable applies SW_B+ to the MIC_HI line (J0401-4), which forward biases Q0404 and asserts the CABLE_DET* input low to the Patriot microprocessor. This tells the processor to switch MUX U0401 to route the BOOT_TX line to J0401-25, rather than the default mode, which routes KEYFAIL* to the pin. This allows the level-shifted BOOT_TX data signal to route directly from the processor's UART port thru U0308 and out J0401-25 to the microphone/programming connector and to the PC.

On the BOOT_RX side, the CABLE_DET* input also drives BOOT_DATA_EN* low, which switches off buffers U0303-4 and U0303-3, routing the level-shifted BOOT_RX data from J0401-26 and to the processor's UART port. This data is level-shifted from 5 V to 2.85 V through U0303-2.

When interfacing with CPS, the TUNER software, and during a flash operation, the control-head display does not go blank. SB9600 messaging continues and, upon removal of the programming cable, the radio usually undergoes a reset operation as part of the normal cable detection and removal process.

High power is different from the mid power radios in several ways. High power is always configured for remote and on the remote TIB there is a GCAI connector instead of a programming port (P104). The GCAI connector is the only USB port on a high power “brick” and unlike mid power, it shares these lines with BOOT_RX and BOOT_TX. For this reason, there is no U0401 MUX and Keyfail is not shared by any other line. The GCAI standard requires that the type of cables are determined by a one-wire memory device, so “CABLE_DET” is not connected to the MIC_HI line. On all radios the default condition of the UART is four-wire RS232 either through the rear J2 connector on mid power or J6 on the TIB of all remote configurations. For this reason, data cables can also be used with CPS. High power does not have a rear connector so the only way to access USB is through the GCAI connector. USB is the default condition of the GCAI, but one-wire is always read any time that a cable is detected.

Programming high power with a GCAI RS232 cable is done the following way. The cable is detected by grounding GP1O0 on the GCAI connector and in turn the processor reads the one-wire memory in the same attached cable. If it determines from one-wire that a two-wire RS232 cable is attached, GCAI_USB-RS232 is lowered to allow 5 volt power on the TIB to supply current to USB_PWR on the GCAI and to turn off the passive FET Q801 which normally allows power to be supplied to the USB interface. On the “brick”, GCAI_USB-RS232 line also drives CABLE_DET and BOOT_DATA_EN*. This line also drives U0303-2, which has now been enabled to receive BOOT_RX on the USB-line. With USB_PWR off U0308 is allowed to drive the BOOT_TX on the USB+ line.

3.8.13 Reflashing/Upgrading Firmware

The FLASH IC is the firmware storage IC. Programming this IC is accomplished using one of the following input paths:

- Two-wire RS-232 directly from a computer’s srial port to the radio’s rear connector data cable HKN6160 (Mid Power only)
- Two-wire RS-232 through an HKN6155 programming cable at the control head’s 10-pin microphone port (Mid Power only)
- Two-wire RS-232 through an HKN6155 programming cable at the Remote Mount Interconnect board’s 10-pin flash port (Mid Power only)
- Two-wire RS-232 through an HKN6183 programming cable at the High Power Remote Mount Interconnect board’s 10-pin GCAI port (High Power only)

For a list of all available programming cables, refer to the table below.

Table 3-17. Programming Cables

Motorola Part Number	Description	Application
HKN6155	Programming Flash Cable	Used with Tuner software, Customer Programming Software (CPS), and FLASHport
RVN4185	Customer Programming Software and Tuner Software	Programming and radio alignment software on CD
HKN6182	High Power GCAI Cable Adapter for Keyloader	Used for keyloading XTL 5000 High Power
HKN6183	High Power GCAI to RS232 Programming Cable	Used for programming XTL 5000 High Power
HKN6184	High Power GCAI to USB Programming Cable	Used for programming XTL 5000 High Power
HKN6122	4-wire data cable, J6 remote TIB	Used for programming XTL 5000
HKN6160	Cable Kit 6’ Dash Mount Data (RS232)	Used for programming XTL 5000 Mid Power

Caution

If you choose to reflash the radio (reflash the IC), DO NOT interrupt the process; otherwise, you might corrupt the FLASH IC and need advanced technical support to revive your radio.

NOTE: In remote-mount configurations, the control head 10-pin microphone port is disabled for any kind of programming.

NOTE: FLASH IC replacement is not supported as a field repair option. If the FLASH IC is removed, the radio cannot be reflashed by a customer or radio depot. This is because the FLASH IC must be hard-boot loaded at the factory to allow the programming of a unique file.

Notes