



## MAINTENANCE MANUAL

## 136-174 MHz SYNTHESIZER/INTERCONNECT BOARD

## 19D900961G13,15 WIDEBAND

## TABLE OF CONTENTS

	<u>Page</u>
DESCRIPTION .....	1
CIRCUIT ANALYSIS .....	1
LEGEND INFORMATION .....	8
OUTLINE DIAGRAM .....	9-10
SCHEMATIC DIAGRAM .....	11-14
PARTS LIST .....	14-17

## DESCRIPTION

The Synthesizer/Interconnect board for the Phoenix-SX two-way radio is microcomputer controlled. A phase locked loop synthesizer generates the transmitter and receiver frequencies in a common voltage controlled oscillator (VCO). The VCO frequency range is approximately 136-174 MHz for transmit, 181-219 MHz for receive.

The microcomputer also controls the generation of Channel Guard tones and codes and provides the carrier control timer in the transmit mode.

It contains interface circuitry for voltage protection and level shifting, an audio processor, a microcomputer, a frequency synthesizer, and an electrically erasable PROM (EE PROM). The EE PROM stores the binary data for the transmit and receive frequencies, Channel Guard tones and codes, and the CCT delay on a per channel basis. A block diagram of the Synthesizer/Interconnect board is shown in Figure 1.

## NOTE

The EE PROM provides the user with the capability to reprogram the EE PROM to meet changing individual system requirements.

Programming for the EE PROM is accomplished by connecting the PROM Programmer to the rear radio connector.

The PROM can then be read or programmed as desired.

Programming information for the EE PROM is included in the instruction manual for the Programmer.

In addition to providing the normal radio functions, the microcomputer has the ability to execute a maintenance diagnostic instruction set to aid in troubleshooting the radio. Further details are included in the Service Section of this manual.

## CIRCUIT ANALYSIS

## CHANNEL SELECT

Frequency selection is controlled by channel select switch S1. When pressed, A- is applied to microcomputer U801-32 (P15 = port 1 bit 5), causing the microcomputer to advance through the selected channels at the rate of 3 Hz until the switch is released. If the switch is pressed for less than 650 ms the channel selected is advanced by one. After the channel displayed reaches the maximum number of channels programmed in the radio, it will automatically roll over and the next channel displayed will be 1.

When the channel select switch is released, the microcomputer applies +5 VDC to the EE PROM through Q802. The frequency bit code corresponding to the channel displayed is then loaded into the synthesizer. If the channel select switch is pressed while the transmitter is keyed, the microcomputer will unkey the transmitter until the channel select switch is released.

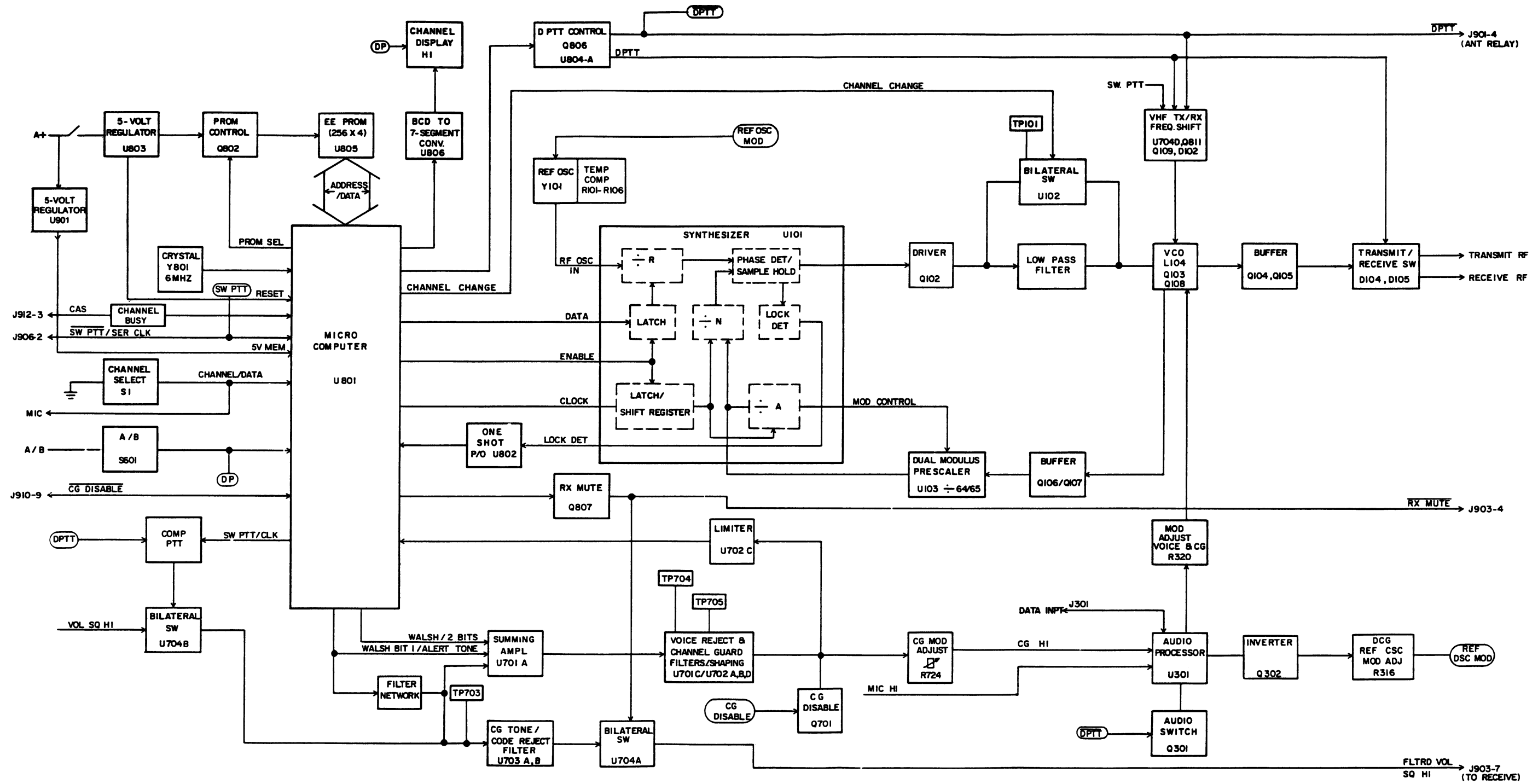


Figure 1 - Block Diagram

RC 4402B

## CHANNEL BUSY INDICATOR

Channel Busy indicator H2 is controlled by the CAS line and is turned on when the selected channel is busy. Hole HL94 is provided to allow the option indicator to be controlled by an alternate signal.

## MODE A/B

Mode A/B switch S601 doubles the channel selection capability of the radio. S601 is located on the transmit/receive board.

Eight address locations are used in the EE PROM for each transmit and receive frequency. The display is capable of displaying channels one through eight. By operating the A/B pushbutton switch the user can select two independent transmit and receive frequencies per channel displayed, providing the radio with up to 16 independent transmit and receive frequencies.

Mode B is indicated by an illuminated decimal point on the 7 segment display. 8.5V CONT is applied to the DP input from the MODE A/B switch on the Tx/Rx board.

The Mode A/B switch may be used to provide mobile-to-mobile communications through an intermediate repeater (repeated path) or direct mobile-to-mobile communications. For example: channel 1 Mode A may be programmed for the repeater frequency (repeated path) while channel 1 Mode B would be programmed for the mobile receive frequency (direct path). Judicious programming will allow selection of repeated or direct communication paths on selected channels.

In single frequency radios the MODE A/B switch is not provided. When the condition exists R914 holds the MODE A/B input to the microcomputer low, preventing it from selecting any other channel. In two frequency radios with MODE A/B switch, the level of the MODE A/B input is controlled by the MODE A/B switch located on the transmit/receive board.

## MICROCOMPUTER CONTROL SYSTEM

The microcomputer responds to the manually initiated functions of Push-to-talk, Channel Select, and Mode A/B. All other operations occur automatically and are controlled by the microcomputer.

When the PTT switch is pressed A- is applied to microcomputer U801-38 from J911-2. The microcomputer immediately mutes the receiver by turning on Q807 which provides a low level to J903-4 to mute the receiver. The microcomputer

then delays 10 milliseconds before loading the synthesizer with the transmit bit code. This allows the audio amplifier to be turned off before the synthesizer frequency is changed. After this delay the microcomputer turns on PROM power switch Q802, applying +5V to EE PROM U805. The transmit bit code is then loaded in parallel from the PROM into the microcomputer and then serially into the frequency synthesizer over the clock and data input lines.

Once the bit stream is loaded into the synthesizer an enable pulse and a 10 millisecond channel change pulse is provided to allow the synthesizer to generate the correct RF frequency. The microcomputer immediately begins monitoring the LOCK DET line to verify that the synthesizer is 'on' frequency. If the synthesizer is not locked on the correct frequency negative pulses will be present on the LOCK DET line and the microcomputer will reload the synthesizer in an attempt to lock it on frequency. If the synthesizer is locked on the correct frequency, the microcomputer will key the transmitter by pulling the input line to inverter U804A low. This allows the output of U804A to rise to +8.5 VDC, forward biasing transmit select diode D104, permitting the synthesizer generated RF frequency to pass through to the exciter through P151. Typical attack time of the transmitter is 50 milliseconds.

At the same time transistor Q806 is turned on, applying DPTT to audio switch Q301. Q301 is also turned off, removing the 'short' from amplifier U301A and enabling the audio processor.

## FREQUENCY SYNTHESIZER

The frequency synthesizer generates the transmit and receive frequencies for all channels under control of the microcomputer. The frequency synthesizer consists of a reference oscillator Y101, synthesizer IC U101, bilateral switch U102, low pass filter, VCO -Q103, and -Q108, buffers -Q104, -Q107, and high speed dual modulus counter U103.

Reference Oscillator

The reference oscillator consists of Y101, a junction FET Q101, varicap D101, tuned coll L101, and associated circuitry. The 5 PPM Colpitts oscillator operates at a frequency of 13.2 MHz. Voltage is provided by the 8.5V continuous supply. A temperature compensation network consisting of R101 thru R106, provides a temperature compensated voltage to varicap D101 to maintain the correct frequency. The temperature compensator, utilizing an inverse DC S-curve output characteristic, varies the output voltage to the varicap as a

function of temperature. The temperature compensation network maintains frequency over a temperature range of  $-30^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$  ( $-22^{\circ}\text{F}$  to  $+140^{\circ}\text{F}$ ). The varicap is also used to modulate the oscillator.

Diode D108 produces a negative DC level at the gate of FET Q101 depending on the amplitude of the oscillations. This, in effect, produces a negative feedback, RF to DC, and prevents the oscillator from going into limiting. Slug tuned coil L101 sets the frequency of the oscillator. Modulation voltage for the reference oscillator is adjusted by R316 in the audio processor and applied to varicap D101 through C101 and R109. R316 adjusts the deviation. Refer to the service section for adjustment procedures.

The synthesizer contains three dividers, a phase detector, two shift registers, and a lock detect circuit. When the PTT switch is pressed (transmit), released (receive), or a different channel selected, new frequency data is received on the clock, data, and enable lines and the synthesizer immediately begins generating the new RF frequency. This serial data determines the VCO frequency by setting the internal dividers. The reference oscillator frequency applied to the programmable divide by R counter is divided down to some lower frequency as indicated by the input data and applied to the internal phase detector.

The phase detector compares this signal with the output of the internal  $\div N$  counter. The output of the  $\div N$  counter is a function of the RF frequency which is divided down by the dual modulus prescaler and the  $\div N$  counter. When operating on the correct frequency the inputs to the phase detector are identical and the output voltage of the phase detector is constant. Under these conditions, the VCO is stabilized or locked on frequency. If the compared frequencies (phases) differ a  $\pm$  error voltage is generated and applied to Q102. This error voltage is then supplied to the VCO through the frequency acquisition circuit and low pass filter. The capacitance of varicaps D106 and D109 vary in accordance with the applied error voltage thereby resetting the VCO to the correct frequency. Capacitor C116 is a holding capacitor to store the 'hold' voltage for the phase detector/sample and hold circuit. C117 is a ramp capacitor which also is part of the sample and hold circuit. The value of C117 determines the rate of charge of the ramp.

The lock detect line provides lock status information to the microcomputer through a one shot (part of U802).

### Acquisition and Low Pass Filter

The output of the synthesizer is applied through buffer Q102 to the low pass filter. The low pass filter consisting of R118-R120, and C119-C121 eliminates undesired pulses on the VCO error control line to provide a constant DC level to frequency adjusting varicaps D106 and D109.

When a channel change pulse is received bilateral switch U102 is turned on to bypass the low pass filter effectively increasing the bandwidth and decreasing channel acquisition time. The channel change pulse is 10 milliseconds wide.

### Voltage Controlled Oscillator VCO

The VCO is a wide range JFET oscillator with an operating range of 136-219 MHz. The frequencies for VHF are 136-174 MHz in transmit and 181-219 MHz in receive. At UHF the transmit frequencies are 150-156.66 MHz with receive frequencies of 165-171.666 MHz. The divided down reference frequency is 5 kHz. A simplified diagram of the VCO is shown in Figure 2. It consists of Q103, Q108, L104, L103, L111, D106, D107, and D109 and associated circuitry. VCO frequency is controlled by an error control voltage from the synthesizer and varicaps D106, D107 and D109. Frequency range centering is provided by L104. Audio modulation is provided by the audio processor and applied to the VCO through C122.

The output of the VCO is taken from the drain of Q103 and applied to RF output buffers Q104 and Q105. These buffers provide drive for receiver injection, transmitter exciter, and feedback buffers Q106 and Q107.

A transmit/receive PIN diode switch, D104 and D105, directs the RF output to the transmitter or receiver. The switch is controlled by the DPTT signal from the microcomputer. When DPTT is high, D104 conducts and RF is fed to the transmitter and to the receiver when DPTT is low allowing D105 to conduct.

### Dual Modulus Counter

The VCO frequency is fed back to dual modulus counter, U103, through buffers Q107 and Q106. The counter divides the VCO frequency by 64 or by 65 depending on the status of the modulus control line. The divided down reference frequency is 4.16 kHz for radios operating in the 450-470 MHz band and 5.0 kHz when operating in the 136-174 MHz band.

The output of the dual modulus counter is applied to the  $\div N$  counter in the synthesizer. It is then divided down and compared in frequency and phase with the divided down frequency from the

## CIRCUIT ANALYSIS

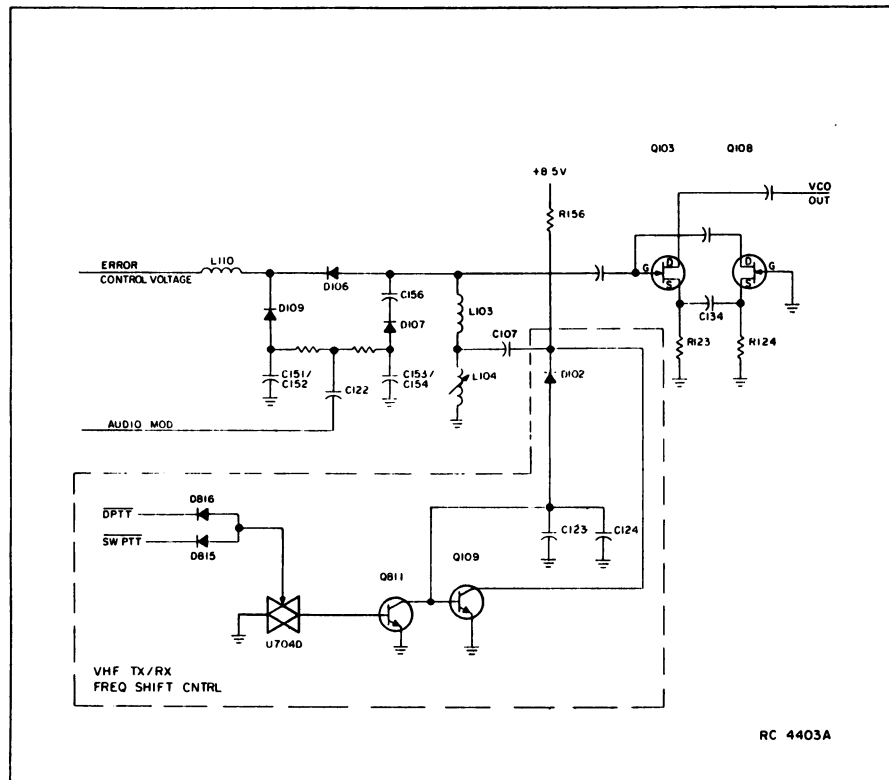


Figure 2 - VCO Simplified Diagram

reference oscillator. The  $\div N$  count is set by the microcomputer.

#### VHF Transmit/Receive Frequency Shift

In VHF radios the VCO frequency is shifted approximately 45 MHz between the transmit and receive modes. The frequency shift is controlled by the PTT circuits. In the transmit mode the VCO operates between 136-174 MHz, while in the receive mode it operates between 181-219 MHz. The Tx/Rx frequency shift circuit is comprised of bilateral switch U704D, Q811, Q109, and diode switch D102. This circuit is operable in VHF radios only and is disabled by removing cable W802 connected between H21 and H22.

In the receive mode the PTT circuits are inactive. U704D is on, Q811 is off, and Q109 is on. Diode switch D102 is forward biased connecting capacitors C123 and C124 across tunable coil L104. These two capacitors provide an AC short across

L104, electrically removing it from the circuit and shifting the VCO operating range to 181-219 MHz.

In the transmit mode the PTT lines are low. U704D is off, Q811 is on, and Q109 is off. Diode switch D102 is reverse biased, electrically disconnecting the AC shorting capacitors (C124 and C123) from across tunable coil L104. This lowers the VCO operating frequency to the 136-174 MHz range.

#### Audio Processor

The audio processor provides audio pre-emphasis with amplitude limiting and post limiter filtering. A total gain of approximately 24 dB is realized through the audio processor. 20 dB is provided by U301B and 4 dB by U301A.

The 8.5 Volt regulator powers the audio processor and applies regulated +8.5V through J903-2 to a voltage divider

consisting of R306 through R309. The +4.25V output from the voltage divider at the junction of R307 and R308 establishes the operating reference point for both operational amplifiers. C305 provides an AC ground at the summing input of both operational amplifiers.

Audio direct from the microphone is coupled to the audio processor through C313 and R302 to the input of operational amplifier U301B-6.

When the input signal to U301B-6 is of a magnitude such that the amplifier output at U301B-7 does not exceed 4 volts P-P, the amplifier provides a nominal 20 dB gain. When the audio signal level exceeds 4 volts peak-to-peak, diodes D301 and D302 conduct on the positive and negative half cycles providing 100% negative feedback to reduce the amplifier gain to 1. This limits the audio amplitude at U301B-7 to 5 volts peak-to-peak.

Resistors R303, R304, R305, and capacitor C302 comprise the audio pre-emphasis network that enhances the signal to noise ratio. R304 and C302 control the pre-emphasis curve below limiting. R305 and C302 control the cut-off point for high frequency pre-emphasis. As high frequencies are attenuated, the gain of U301B is increased.

The amplified output of U301B is coupled through C307, R313 and R314 to a second operational amplifier U307A.

The Channel Guard tone and data inputs are applied to U301A-2. The CG tone (or data) is then combined with the microphone audio.

A post limiter filter consisting of R314, R313, R315, C308 and C309 provide 12 dB per octave roll-off. R313 and C307 provide an additional 6 dB per octave roll-off for a total of 18 dB.

#### SERVICE NOTE

R313-R315 are 1% resistors. This tolerance must be maintained to assure proper operation of the post limiter filter. Use exact replacements.

The audio processor output is coupled through J302 to the transmitter. R316 and R320 are output level adjustment controls to set the modulation sensitivity for the VCO and reference oscillator.

Shorting switch Q301 is turned on in the receive mode (DPTT is high) to short out U301-A and prevent any interference from the transmit audio circuits.

#### CHANNEL GUARD

Channel Guard provides a means of restricting calls to specific radios through the use of a continuous tone coded squelch system (CTCSS) or a continuous digital coded system (CDCSS). Tone frequencies range from 71.9 Hz to 210.7 Hz. There are 83 standard programmable digital codes. The Channel Guard tone frequencies and digital codes are software programmable. Both tone frequencies and digital codes may be used simultaneously. These codes and frequencies are listed in the Programmers Manual.

The microcomputer selects the assigned code/tone information from the EE PROM memory for each channel, transmit and receive, and generates the Channel Guard signal. This signal is applied as Walsh Bit 1 and 2 to summing amplifier U701A. These two bits are summed together and filtered to provide a smooth sine wave for tone Channel Guard. For CDCSS Channel Guard units, walsh bit 2 is used to generate squarewaves.

The switched volume/squelch Hi signal to the summing amplifier is controlled by bilateral switch U704B. In the encode mode COMB DPTT is low turning U704B off and preventing any input from the SW Vol/Sq Hi line from interfering with the encoding signal.

The output of summing amplifier U701A is applied to buffer/amplifier U702B through a two-pole active voice reject filter consisting of U701B and C and U702A and D. The active filter shunts all frequencies above 300 Hz to ground, thereby preventing those frequencies from interfering with the encoded signal. The output of U702B is the assigned CG tone or digital signal. This signal is applied to the audio processor through CG deviation control R724. Channel Guard deviation is set for 0.75 kHz.

#### CG Decode

In the decode mode, COMB DPTT is high. U704B is turned on and audio from the SW Vol/Sq Hi line is applied to summing amplifier U701A through bilateral switch U704B. This signal is amplified and filtered by U701A, B, C and U702A, B and D, so that only the CG signal (if present) is applied to hard limiter U702C. The CG signal is squared up for comparison by the microcomputer to determine if the CG signal is correct. If the microcomputer determines the CG signal to be correct, RX Mute transistor Q807 is turned off. The Rx Mute line is pulled high by pull up resistor R715. This turns on bilateral switch U704A and allows the audio on the FLTRD VOL/SQ HI line to pass through to the receiver.

## CHANNEL GUARD (CG) DISABLE

The CG DIS line has a double function. It can disable the encode or the decode CG function. The encode disable function is controlled by the PTT switch while the decode function is disabled within the microcomputer software. To disable the decoder, the CG DIS/SER CONTL line should be grounded. The microcomputer will detect that the line is low, and turn RX MUTE transistor Q807 off. The decode filter/limiter circuit is not affected, it continues to operate. The detection software also does not stop working. This allows the off hook STE to function.

When the CG DIS line is pulled high (>8.5V), the microcomputer does not sense any changes. It is buffered by protection diode D810. Channel Guard disable transistor Q701 will turn on when the CG DIS line goes above 8.5 V and shorts the output of the filter to ground. This disables the encoder by preventing any signal from going out on CG HI and will also disable the decoder since no limited CG tone will go to the microcomputer. The receiver will be muted since no CG is decoded. Disabling the decoder this way will never allow the audio to open up, while taking the radio off hook (pulling CG DIS low) will always make the radio open up. Turning CG Disable transistor Q701 on causes the DC bias to change. It will take 2 or 3 seconds for the bias to restore itself after the encoder is disabled.

## SQUELCH TAIL ELIMINATION (STE)

STE eliminates squelch tails when the radio is on hook or off hook. When Channel Guard is disabled (off hook) the decoder is still looking at the received signal. The RX MUTE line is high, as would be normally expected. The Channel Guard decoder is looking for the STE burst (phase reversal in tone Channel Guard, STE tone in Digital Channel Guard.) If an STE burst is detected, the RX MUTE line will go low for about 200 ms. This will prevent the squelch tail from being heard. After 200 ms, the RX MUTE line will go high again; by now the transmission has ended and the squelch will hold the audio closed. The off hook STE does not affect the operation of the Channel Guard while on hook. Another way of looking at it: the radio will go quiet for 200 ms any time STE is detected. If it was on hook it will stay quiet after the 200 ms, if it was off hook it will

revert to noise squelch operation. STE operates only on the tone the radio is programmed to receive. If the signal has a Channel Guard tone the radio is not programmed to receive and the microphone is off-hook, STE will not be active. CDCSS STE works regardless of the code.

## DATA POLARITY INVERSION

In some instances it is necessary to invert the polarity of the digital Channel Guard signal to enhance system compatibility. Inverted polarity normally results in a wrong code or one that cannot be used. When this occurs, restrap jumper cable W701 connected between HL70 and HL69 to HL70 and HL66.

## CARRIER CONTROL TIMER

The Carrier Control Timer (CCT) is contained within and controlled by the microcomputer. Each time the PTT switch is activated, an internal counter begins to count down. If the counter times out, the transmitter is unkeyed and a 100 mV rms, 1 kHz tone is sounded until the microphone is unkeyed. The CCT is set for 1 minute.

## CHANNEL MEMORY

When power is removed, channel information from the microcomputer is loaded into the EEPROM to be stored until the power is turned on again. When power is restored, U803 provides a reset pulse to the microcomputer to recall channel information stored in the EEPROM.

5 Volt Regulator

Voltage regulator U803 supplies a regulated +5 VDC to the microprocessor and logic circuitry. The regulator also provides sensing of the output voltage and generation of a RESET signal whenever the output falls out of regulation. C817 delays the reset for approximately 10 ms after voltage stabilizes during power up sequence.

Voltage regulator U901 supplies continuous +5 VDC to the microprocessor memory to maintain PSLM and 128 channel control panel information when unit is powered off.

U901 supplies +5 VDC for memory back-up to the masked microprocessor. On previous groups the memory back-up voltage was supplied from a regulator on the PSLM Board or Mode Expander Board.



**GE Mobile Communications**

General Electric Company  
Lynchburg, Virginia 24502

Printed in U.S.A.

TABLE OF CONTENTS

NOTES & CHARTS-----1 SHEET

SYSTEM-----2

FUNCTION	CPNT SERIES
CG TONE REJECT FILTER	700
5V REGULATOR	800
SYSTEM	900

SYSTEM/REF OSC-----3

FUNCTION	CPNT SERIES
SYNTHESIZER REF OSC	100
TX AUDIO PROCESSOR	300
SYSTEM CONTROL	800
SYSTEM	900

SYNTHESIZER/C.G.-----4

FUNCTION	CPNT SERIES
SYNTHESIZER	100
CHANNEL GUARD	700

SYSTEM-----5

FUNCTION	CPNT SERIES
MICROCOMPUTER CONTROL	800
MULTI FREQ DISPLAY	A901

DEVICE	5V PIN NO	0.5V CONT PIN NO	0.5V SYN PIN NO	GND PIN NO
U102			14	7
U301		8		4
U701		4		11, 12, 13
U702		4		11
U703		8		4
U704		14		7
U804	14			7

SPARE IC FUNCTION

DEVICE	INPUT PIN NO	OUTPUT PIN NO
U701-D	12, 13	14

ALL CHIP RESISTORS ARE 1/8 WATT.  
 ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED.  
 RESISTOR VALUES IN  $\Omega$  UNLESS FOLLOWED BY MULTIPLIER K, OR M.  
 CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER  $\mu$ , n OR, p.  
 INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m, n OR u.

COMPONENT IDENTIFICATION		
PART	GP13	GP15
C125	150-174 MHZ	136-153 MHZ
L103	150p	27p
L104	0.025uH	0.033uH
L104	19B800962P111	19B800962P112

MODEL NO.	REV. LETTER
19D900961G13	D
19D900961G15	D

NOTES:

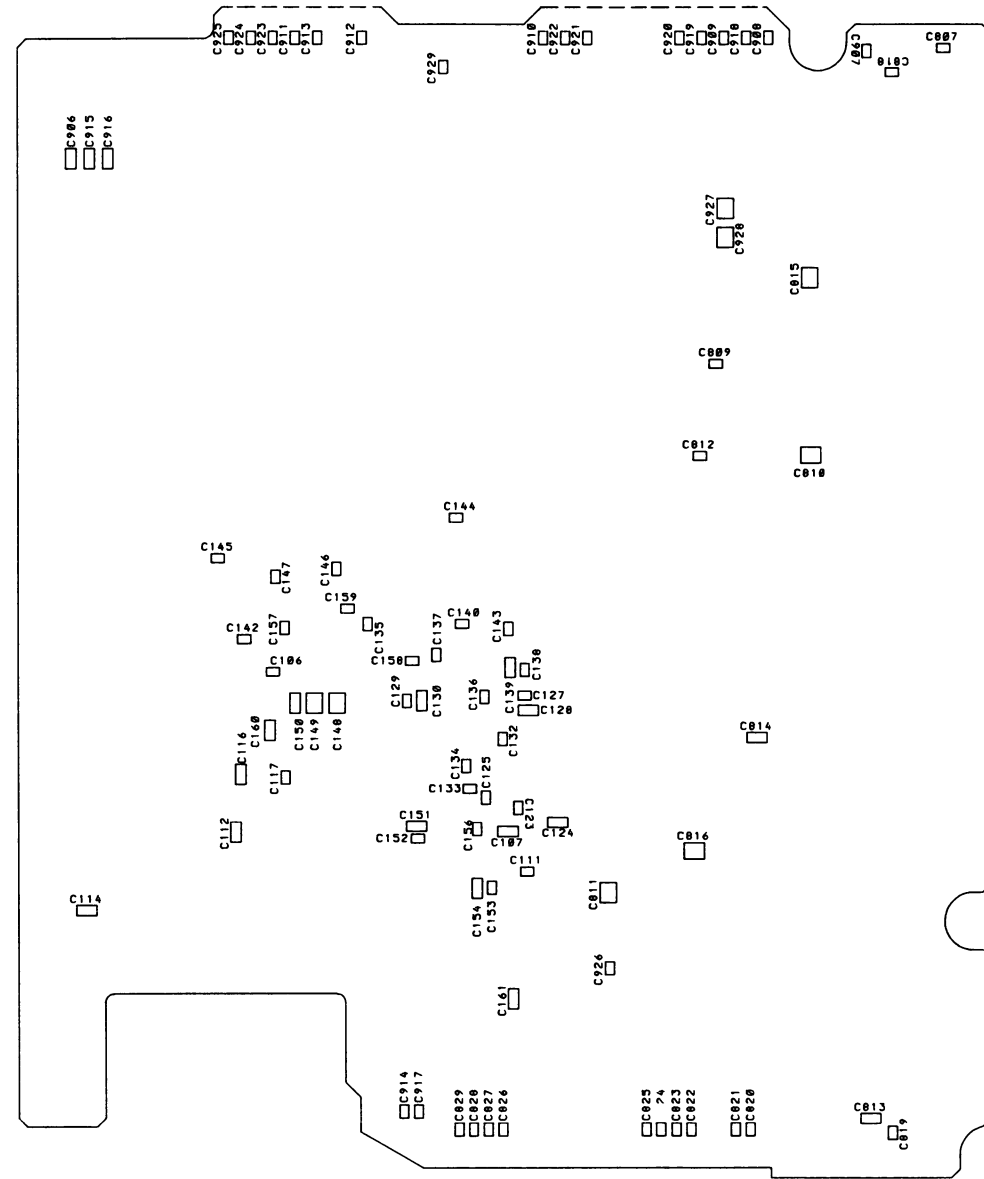
- ⚠ FOR T99 DECODER, ADD JUMPERS HL7 TO HL9, HL12 TO HL14, HL39 TO HL40, HL48 TO HL60, HL19 TO HL55. OMIT JUMPERS W905, W909, W908, W907.
- ⚠ FOR PUBLIC ADDRESS OPTION, ADD JUMPERS HL60 TO HL48, HL3 TO HL4, HL8 TO HL9, HL12 TO HL14. OMIT JUMPERS W902, W906, W904, W908
- ⚠ FOR USING UV ERASABLE U801 (8749) REMOVE W911 AND ADD JUMPER BETWEEN HL31 AND HL32. IF CHANNEL MEMORY IS ALSO DESIRED WITH 8749 (200ma CONTINUOUS BATTERY DRAIN) ADD INSULATED JUMPER BETWEEN HL63 TO HL64 AND OMIT W801.
- ⚠ FOR IGNITION SWITCH CONTROL, REMOVE JUMPER W901.
- ⚠ FOR SPEAKER MUTE FUNCTION WITH THE UNIVERSAL TONE CABLE OPTION WITHOUT PA OPTION, OMIT JUMPER W903, ADD JUMPER HL5 TO HL6 (NOT COMPATIBLE WITH INTERNAL/EXTERNAL SPEAKER). WITH PA OPTION, OMIT W903 ONLY.
- ⚠ FOR EXTERNAL SPEAKER OPTION, REMOVE JUMPER W903 TO DISABLE THE INTERNAL SPEAKER.
- ⚠ PRESENT FOR UNITS WITHOUT MULTI-FREQ DISPLAY.
- ⚠ PART OF KIT PL19A701522.
- ⚠ PWB HAS PROVISION FOR MOUNTING COMPONENTS SHOWN DASHED.
- 11. # DENOTES CHIP COMPONENTS (EXAMPLE R1#), WHICH ARE LOCATED ON SOLDER SIDE OF PWB.
- 12.  $\perp$  DENOTES A- COMMON TO CHASSIS.
- ⚠ FOR PHOENIX INTERNATIONAL, ADD JUMPERS HL24 TO HL60, HL40 TO HL39, HL4 TO R302, HL14 TO HL48. REMOVE W905, D815 AND C713.
- ⚠ THE FOLLOWING JUMPERS ARE IMPLEMENTED USING ONE OHM RESISTORS. W701, W801, W802, W904, W905, W906, W907, W908 AND W909. CLIP BOTH LEADS TO REMOVE JUMPER.
- ⚠ THE FOLLOWING JUMPERS ARE IMPLEMENTED USING ZERO OHM "RESISTORS". W901, W902, W903 W911 AND W912. CLIP BOTH LEADS TO REMOVE JUMPER.
- ⚠ CHANNEL MEMORY VOLTAGE IS SUPPLIED STANDARD FOR MASKED MICROPROCESSORS. CABLE PREVIOUSLY CONNECTED FROM PSLM BD. TO J810 AND J811 ON SYNTH/INTR. BD. NO LONGER REQUIRED.
- ⚠ FOR INTERNAL/EXTERNAL SPEAKER OPTION WITH SWITCH (EXTERNAL TO RADIO) DELETE W903 AND ADD JUMPER HL5 TO HL6.
- ⚠ WHEN T99 OPTION OR PUBLIC ADDRESS OPTION ARE PRESENT WITH MULTI-FREQ DISPLAY, REMOVE R911 AND R8.

LEGEND INFORMATION

Synthesizer/Interconnect & Display Board



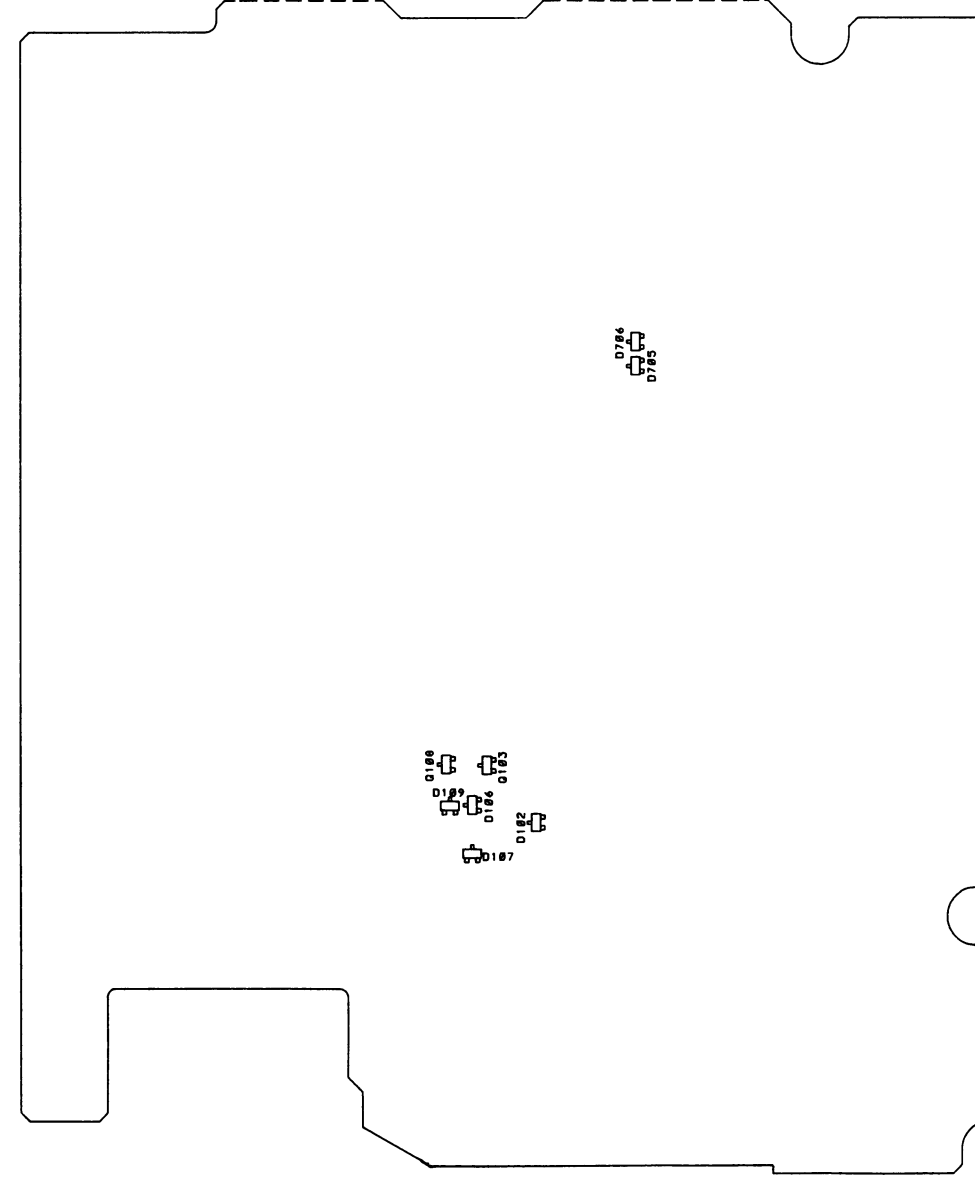
CHIP CAPACITOR  
LOCATIONS



BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 10, Rev. 2)

CHIP TRANSISTOR, DIODE  
LOCATIONS

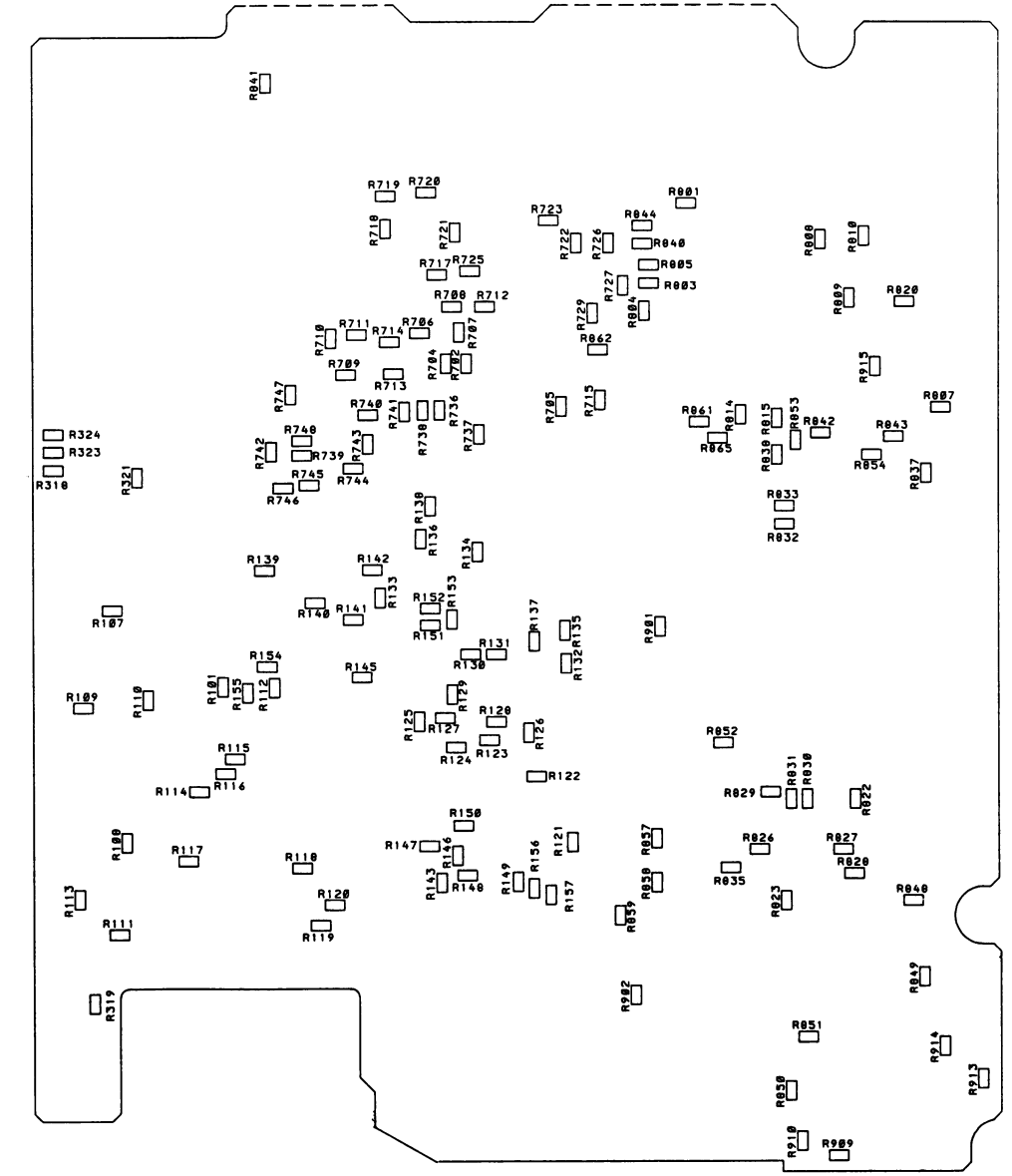


BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 11, Rev. 2)

CHIP RESISTOR  
LOCATIONS

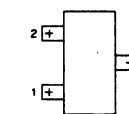
LBI-31733



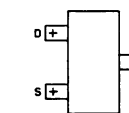
BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 12, Rev. 1)

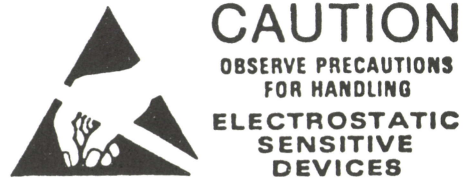
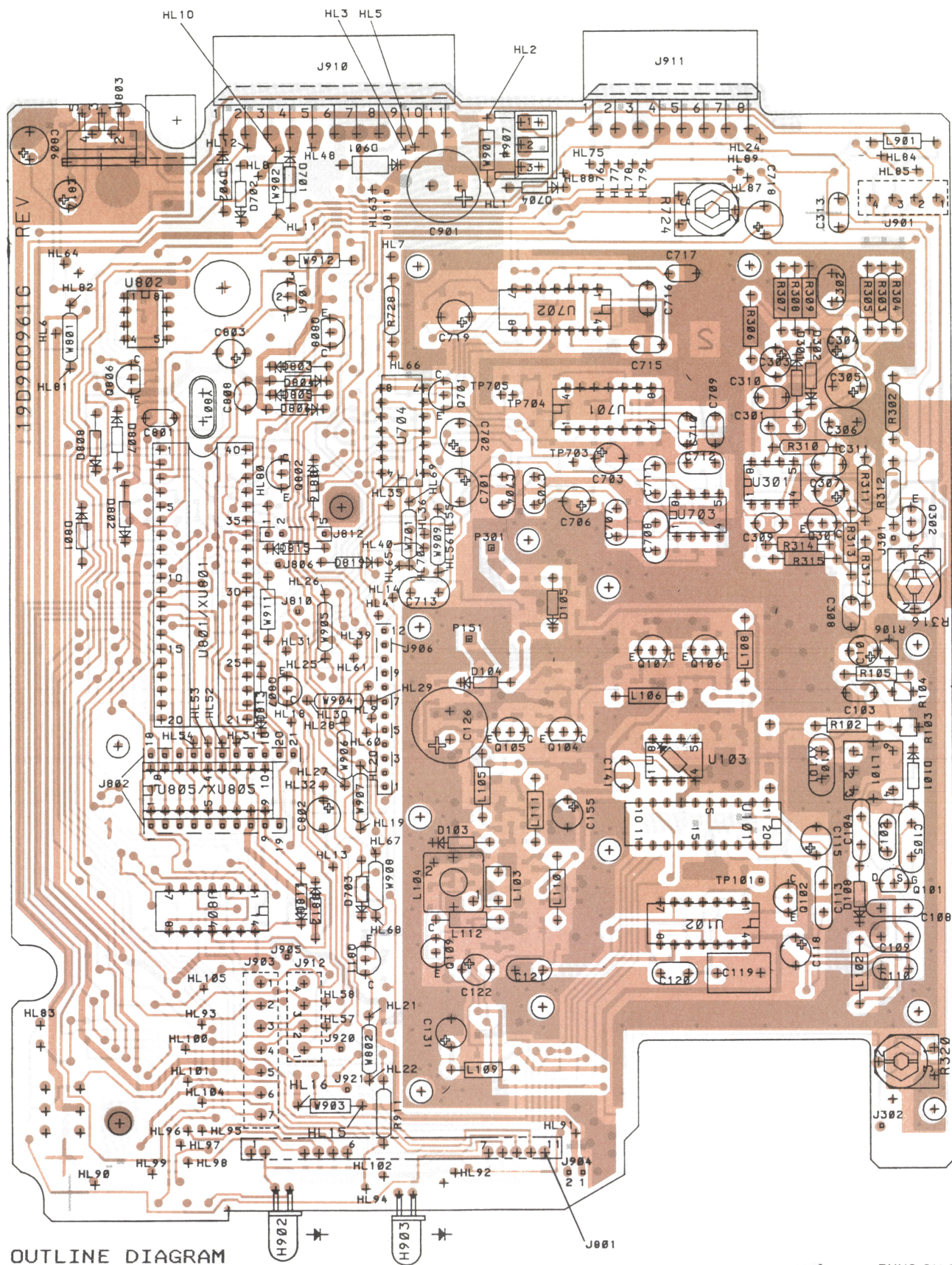
LEAD IDENTIFICATION FOR  
(SOT) DIODES  
(TOP VIEW)



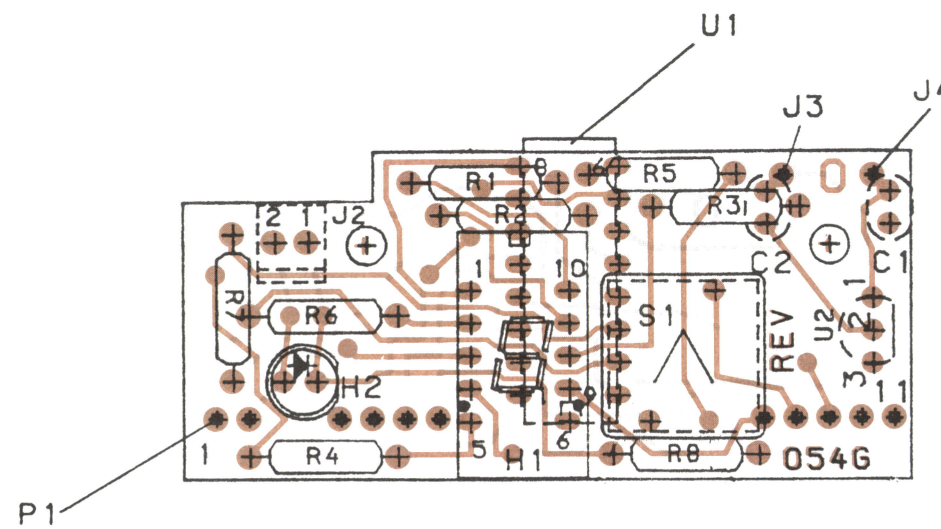
LEAD IDENTIFICATION FOR  
(SOT) TRANSISTORS  
(TOP VIEW)



OUTLINE DIAGRAM  
Chip Component Location



DISPLAY BOARD

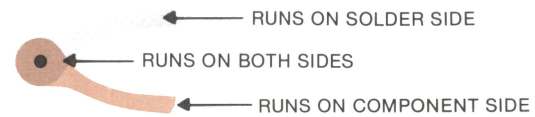


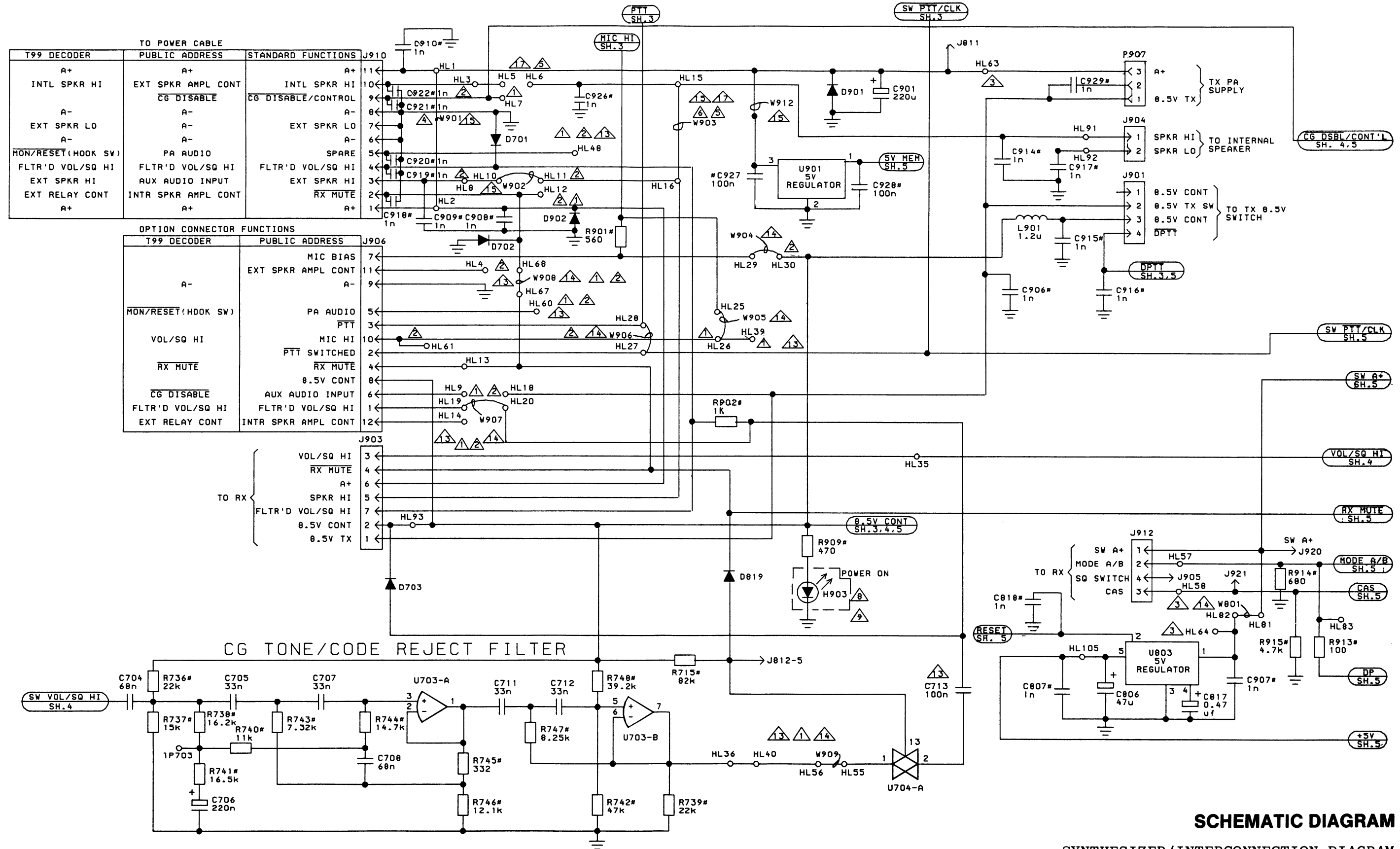
(19D901054, Sh. 1, Rev. 3)  
 (19A703382, Sh. 1, Rev. 0)  
 (19A703382, Sh. 2, Rev. 0)

OUTLINE DIAGRAM

Synthesizer/Interconnect & Display Board

(19D900961, Sh. 10, Rev. 3)  
 (19A704979, Sh. 1 & 2, Rev. 1)  
 (19A704979, Sh. 3 & 4, Rev. 2)

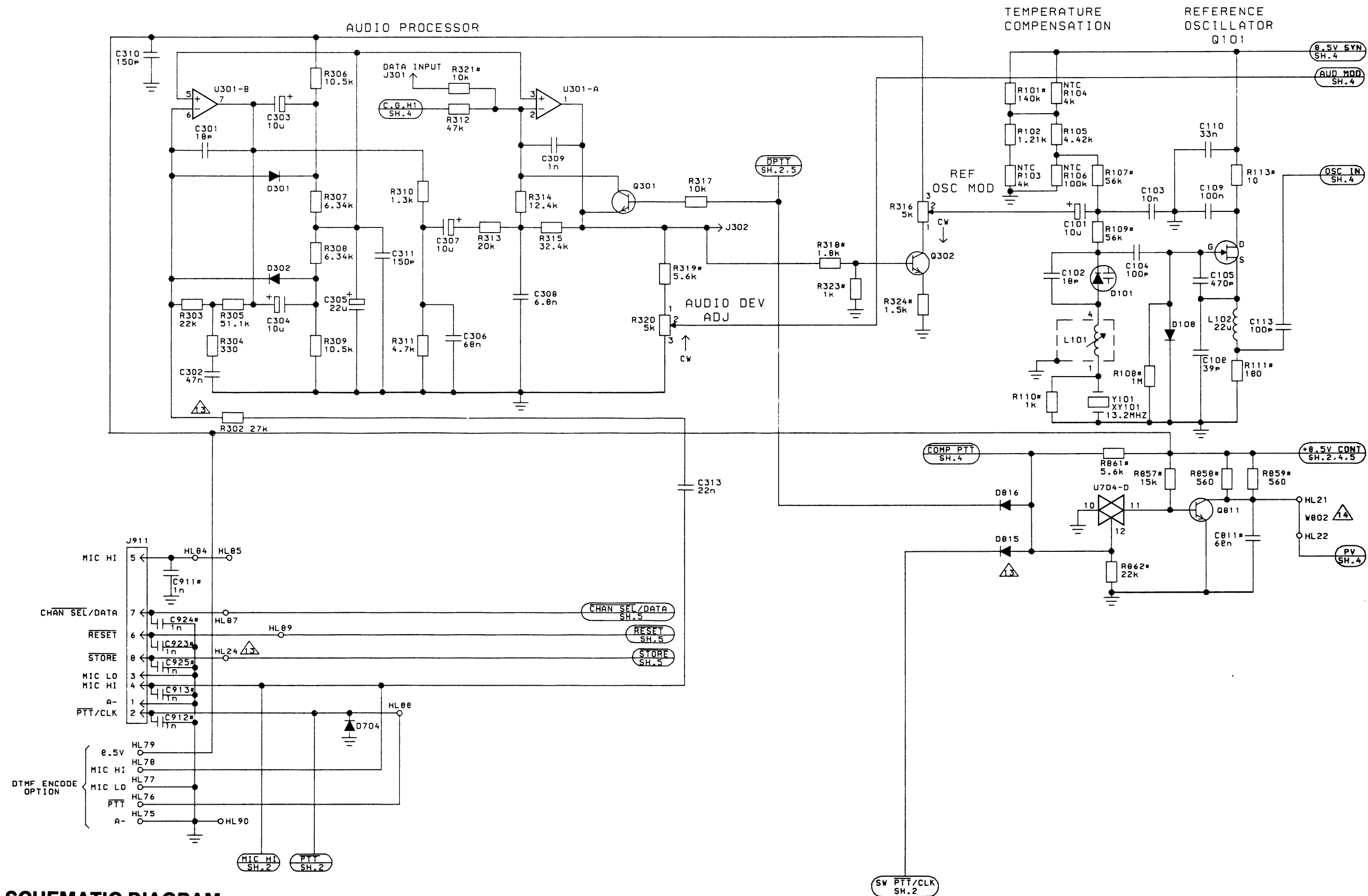




**SCHEMATIC DIAGRAM**

SYNTHESIZER/INTERCONNECTION DIAGRAM  
INTERFACE AND CHANNEL GUARD FILTER

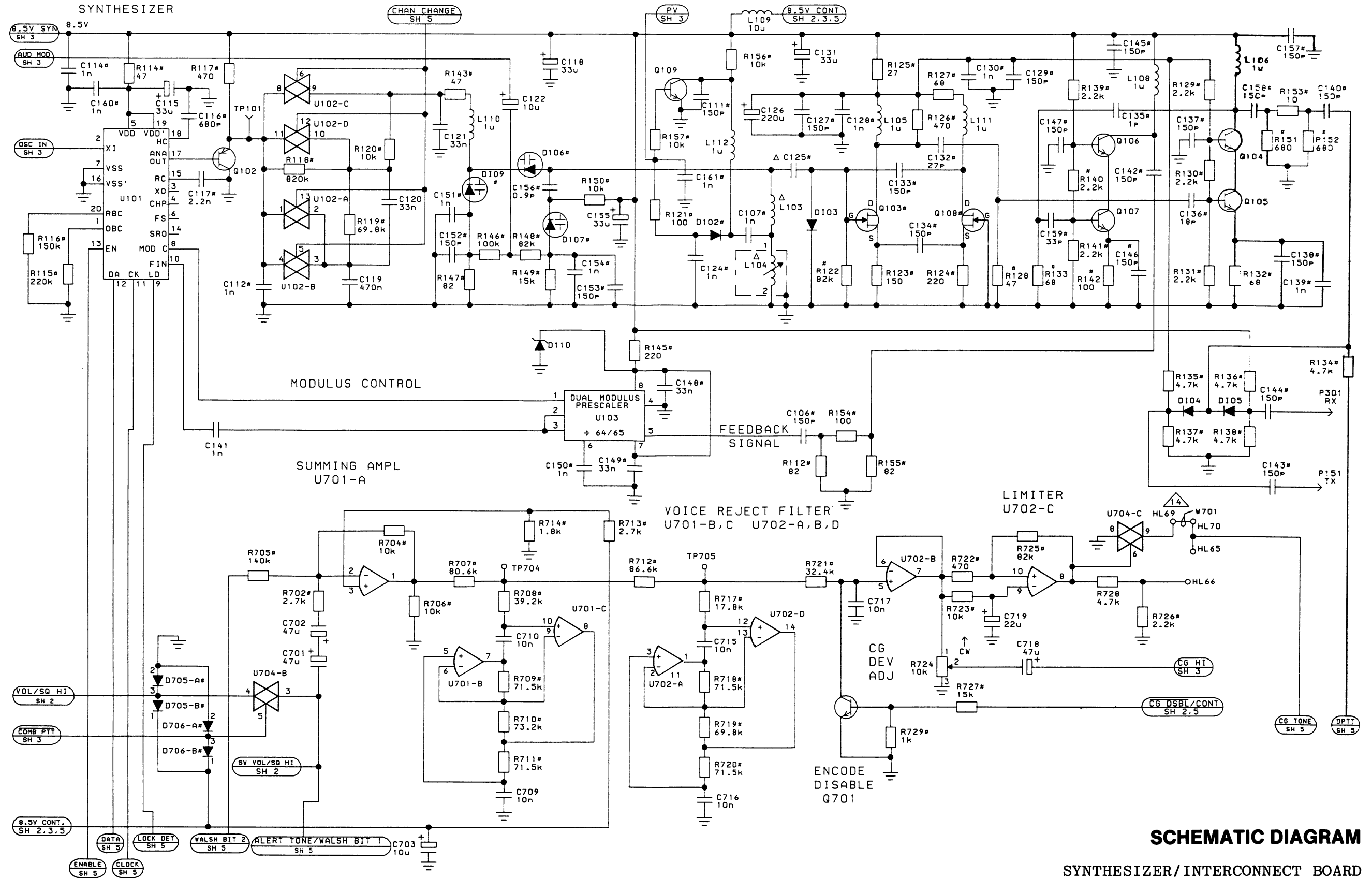
(19D901767, Sh. 2, Rev. 1)



**SCHEMATIC DIAGRAM**

SYNTHESIZER/INTERCONNECT BOARD  
 TRANSMITTER AUDIO AND  
 REFERENCE OSCILLATOR

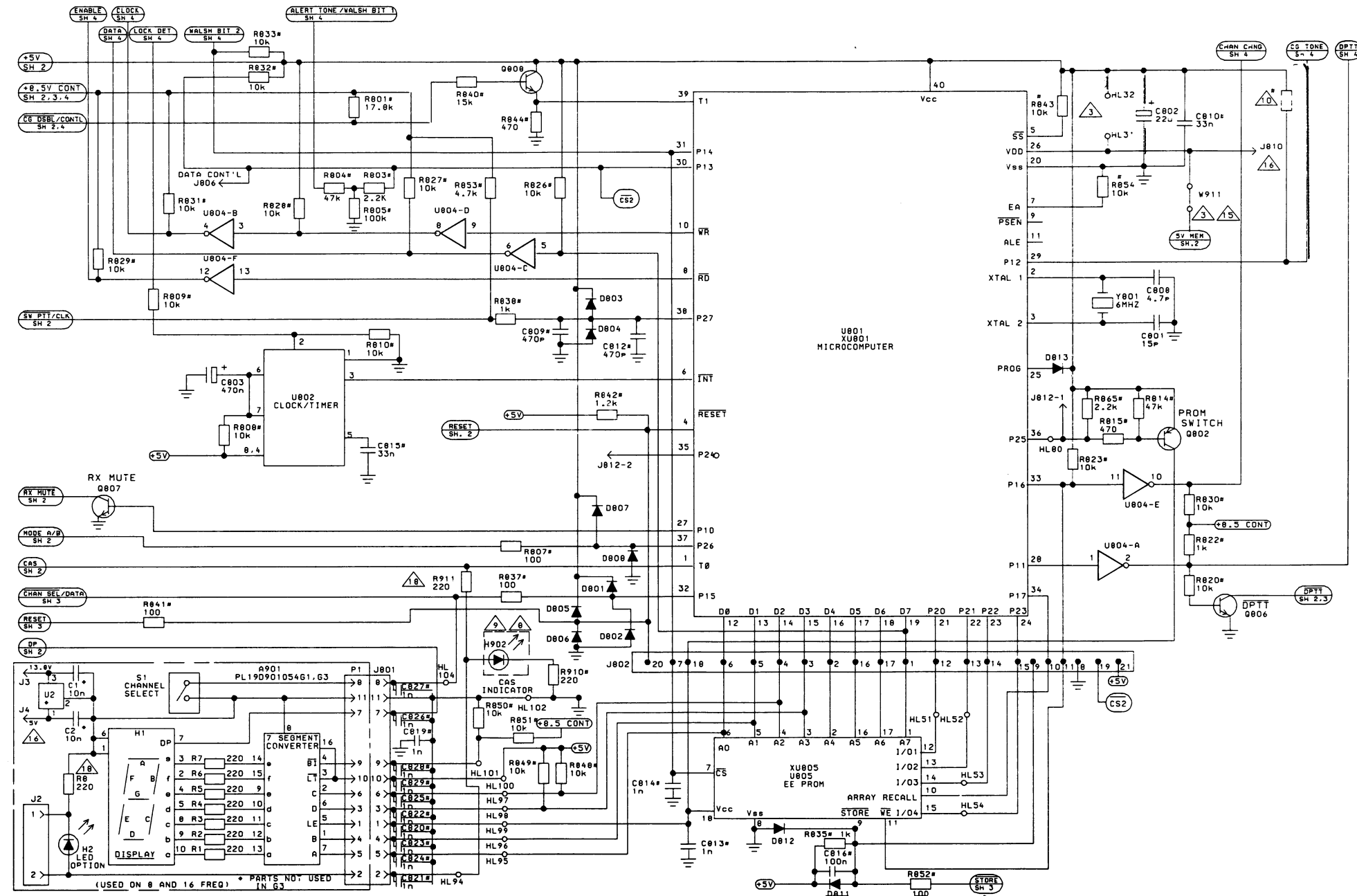
(19D901767, Sh. 3, Rev. 1)



**SCHEMATIC DIAGRAM**

SYNTHESIZER/INTERCONNECT BOARD  
FREQUENCY SYNTHESIZER AND  
CHANNEL GUARD

(19D901767, Sh. 4, Rev. 2)



(19D901767, Sh. 5, Rev. 2)

**SCHEMATIC DIAGRAM**

Synthesizer/Interconnect Board  
System Control & Display Board

SYMBOL	GE PART NO.	DESCRIPTION
C1 and C2	19A700121P6	----- CAPACITORS ----- Ceramic: 0.1 uF ±20%, 50 VDCW. (Used in G1).
H1	19A134712P5	----- LEDES ----- Optoelectronic display: green; sim to HOSP 3603.
H2	19A134354P9	Optoelectronic: yellow; sim to H.P. HLMP4719.
J2	19A700072P28	----- JACKS ----- Printed wire: 2 contacts rated @ 2.5 amps; sim to Molex 22-27-2021. (Used in G1).
J3 and J4	19A703248P1	Contact, electrical.
P1	19A703248P3	----- PLUGS ----- Contact, electrical. (Quantity of 11).
R1 thru R8	H212CRP122C	----- RESISTORS ----- Deposited carbon: 220 ohms ±5%, 1/4 w.
S1	19A701324P2	----- SWITCHES ----- Pushbutton: sim to IEE/Schadow Series MDP Module.
U1	19A700029P204	----- INTEGRATED CIRCUITS ----- Digital: BCD-to-SEVEN segment latch/decoder/driver.
U2	19J706031P1	Linear: Positive 5 volt regulator. (Used in G1).
	19C850665P1	----- MISCELLANEOUS ----- Pushbutton. (Used with S1).
	19A704859P1	Nameplate. (Used on S1).

\*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES







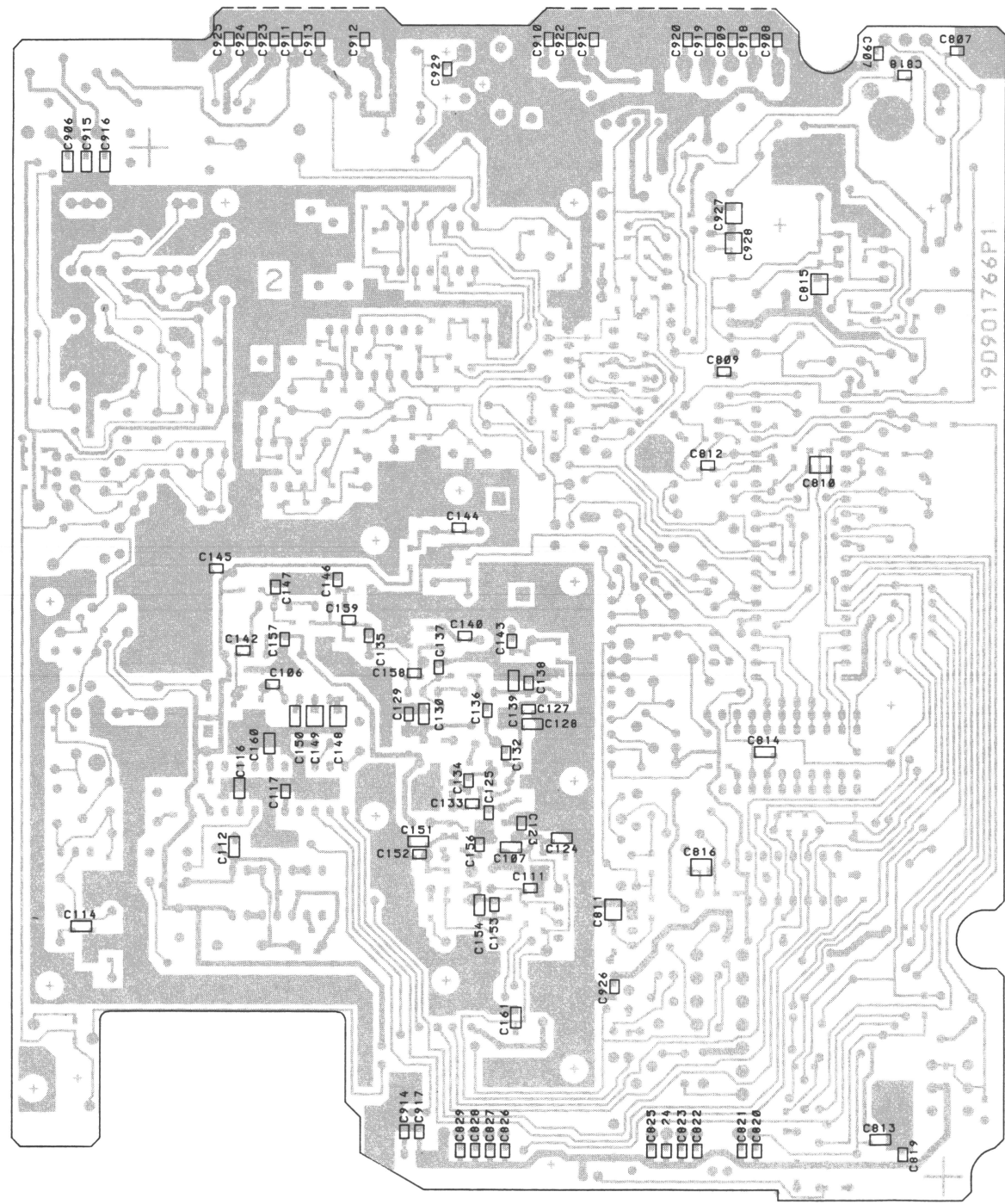
SYMBOL	GE PART NO.	DESCRIPTION
		----- LEDS -----
H902	19A134354P9	Optoelectronic: Yellow.
H903	19A134354P3	Optoelectronic: Green.
		----- JACKS -----
J901	19A116659P185	Connector: 4 contacts rated @ 7 amps; sim to Molex 09-80-1045.
J903	19A116659P186	Connector: 7 contacts rated @ 7 amps; sim to Molex 09-80-1075.
J904 thru J905	19A703248P17	Contact: electrical.
J906	19A703248P15	Contact: electrical. (Quantity of 12).
J910	19A116659P184	Connector: printed wiring, 11 contacts; sim to Molex 09-75-1116.
J911	19A116659P183	Connector: printed wiring, 8 contacts; sim to Molex 09-75-1086.
J912	19A116659P185	Connector: 4 contacts rated @ 7 amps; sim to Molex 09-80-1045.
J920 and J921	19A703248P17	Contact: electrical.
		----- INDUCTORS -----
L901	H343CLP12922	Coil, RF: 1.2 uH $\pm 10\%$ .
		----- PLUGS -----
P907	19A700102P10	Printed wire: 3 contacts; sim to Molex 09-52-3032.
		----- RESISTORS -----
R901	19B800607P561	Metal film: 560 ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R902	19B800607P102	Metal film: 1K ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R909	19B800607P471	Metal film: 470 ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R910	19B800607P221	Metal film: 220 ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R911	H212CRP122C	Deposited carbon: 220 ohms $\pm 5\%$ , 1/4 w.
R913	19B800607P101	Metal film: 100 ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R914	19B800607P681	Metal film: 680 ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
R915	19B800607P472	Metal film: 4.7K ohms $\pm 5\%$ , 200 VDCW, 1/8 w.
		----- INTEGRATED CIRCUITS -----
U901	19A704971P1	Linear: 5 volt Voltage Regulator; sim to Motorola MC78L05ACP.
		----- JUMPERS -----
W901 thru W903	19A700184P1	Jumper.
W904 thru W909	H212CRP910C	Deposited carbon: 1 ohm $\pm 5\%$ , 1/4 w.
W911 and W912	19A700184P1	Jumper.

**PRODUCTION CHANGES**

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

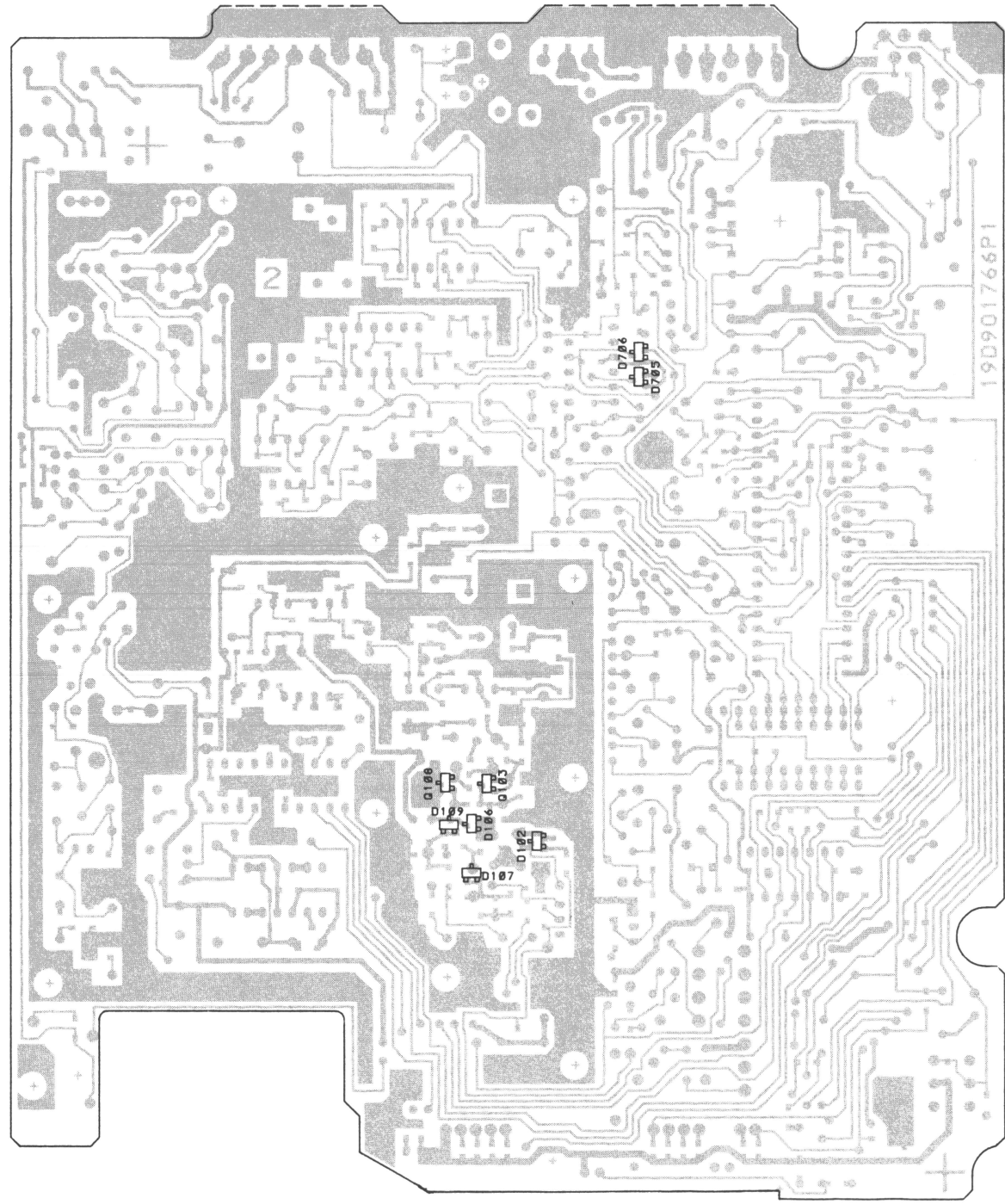
- REV. A - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G13~~  
~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G15~~  
To improve operation and increase synthesizer bandwidth, deleted C123.  
C123 was: 19A702061P65 Ceramic: 150 pF  $\pm 5\%$ , 50 VDCW.
- REV. B - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G15~~  
To improve VCO operation, changed L103.  
L103 was: 19B800891P3 Coil, RF Choke.
- REV. B - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G13~~  
REV. C - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G15~~  
To improve regulator operation, added D110 zener diode.
- REV. C - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G13~~  
REV. D - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G15~~  
To enhance transmitter operation, changed C313 & R302.  
C313 was: T644ACP310K Polyester: .010 uF  $\pm 10\%$ , 50 VDCW.  
R302 was: H212CRP356C Deposited carbon: 56K ohms  $\pm 5\%$ .
- REV. D - ~~SYNTHESIZER/INTERCONNECT BOARD 19D900961G13~~  
To improve deviation flatness, changed D109.  
D109 was: 19A700085P2 Silicon: sim to MMBV109.

This addendum adds the OUTLINE DIAGRAMS for the CHIP COMPONENT LOCATIONS with the solder side printed wire patterns.



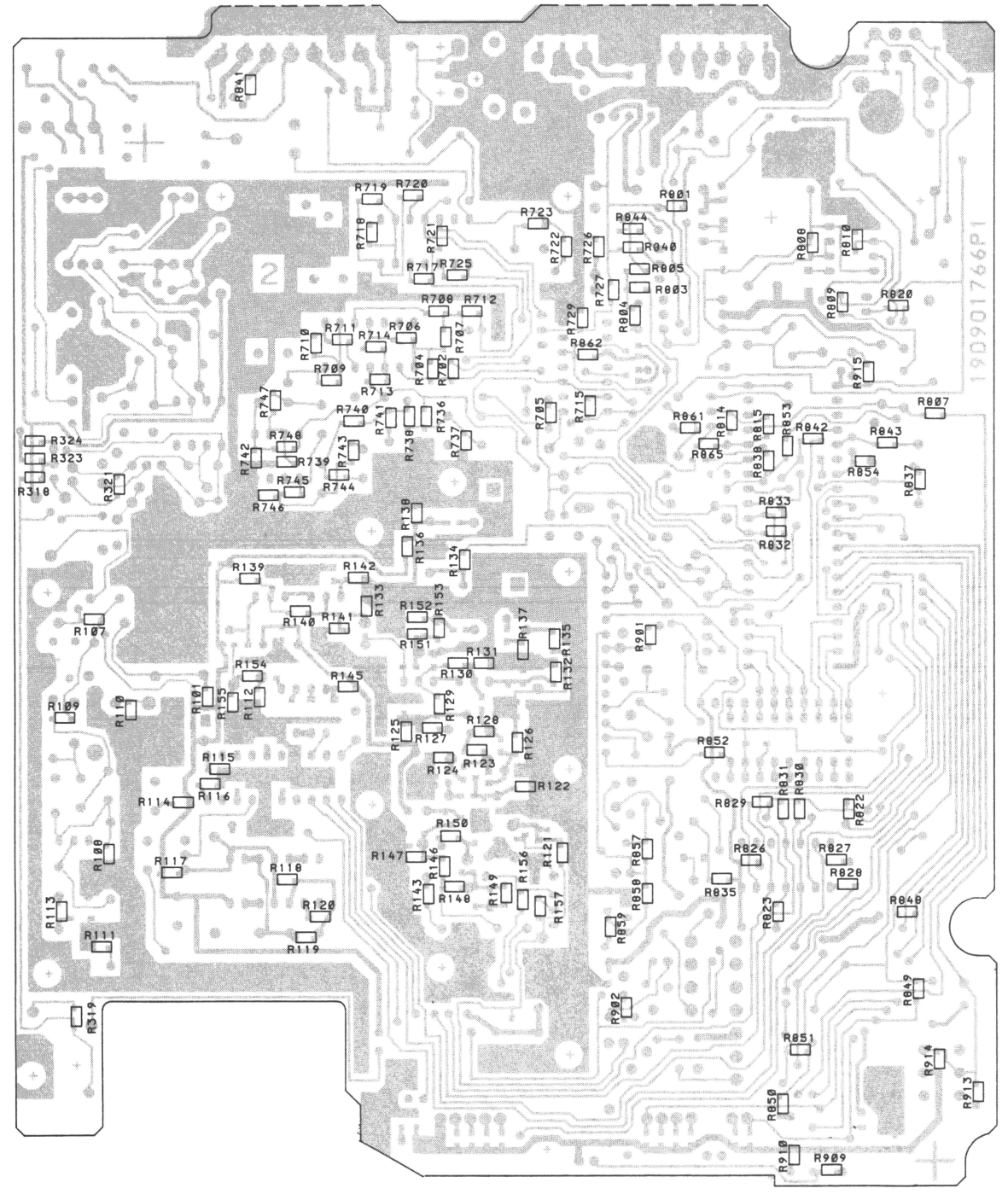
BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 10, Rev. 2)  
(19A704979, Sh. 3 & 4, Rev. 2)



BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 11, Rev. 2)  
(19A704979, Sh. 3 & 4, Rev. 2)



BACK VIEW OF COMPONENT BOARD

(19D900961, Sh. 12, Rev. 1)  
(19A704979, Sh. 3 & 4, Rev. 2)