ERICSSON ⊰ | GE

MAINTENANCE MANUAL
LOGIC BOARD 19D901690G5
FOR MVS

L
O
G
I
C

TABLE OF CONTENTS

DESCRIPTION

The Logic Board (A1) controls the main operation of the MVS radio.

It is located in the bottom of the frame assembly underneath the Audio Board. Refer to the combination manual for a complete mechanical layout of the board. Figure 1 provides a Block Diagram of the Logic Board. Refer to the Table of Contents in this publication for IC data sheets with pinout information on integrated circuits and modules.

The Logic Board contains a microprocessor and associated memory circuits which include an EPROM of controlling the processor and a programmable "personality" EEPROM to store customer frequencies, tones and options. Programmable data is entered using an IBM compatible personal computer and a RS-232 interface. Refer to the programming manual for programming instructions.

CIRCUIT ANALYSIS

MICROPROCESSOR

Microprocessor U701 is an 8-bit processor that performs the logic functions to provide the control signals required in the radio. An external 11.0592 MHz crystal (Y701) is used for the clock. The microprocessor controls the following:

- Synthesizer

- Transmit circuit

- Decoding of Channel Guard (tone or digital) and Type 99 tones

- Generation of Channel Guard (tone or digital)

- Transmitter and receiver audio mute gates.

Serial data at a 300 baud rate is used for communication between the microprocessor and the Front Cap Assembly. U701 uses the KEYPAD SERIAL line to receive Control Panel commands from the microprocessor in the Front Cap Assembly. U701 sends data back on the DISPLAY SERIAL line to update the LCD. Both serial lines normally rest at 5 volts with the data causing the lines to go low.

Diodes D701-D708 on $\overline{PTT}$, the serial lines, and AUDIO MUTE protect the microprocessor from static discharges. These lines are pulled high to +5 volts through 50K ohm resistors inside the microprocessor.

ERASABLE PROM (EPROM)

EPROM U703 is CMOS 8K byte device with an internal address latch. All information required by the microprocessor for system operation resides in this EPROM.

ELECTRICALLY ERASABLE PROM (EEPROM)

EEPROM U704 is a 512 x 8-bit memory device, designated the "personality" PROM This personality PROM stores all required customer information which includes: Frequencies, Tones, and Options. The EEPROM also retains the status of all radio functions (channel selection, volume setting, scan channel list, and scan on-off function) to return the radio to the same mode of operation after power is turned off or removed from the radio.

DC power for U704 is switched by transistor Q705. During the active high reset pulse to the microprocessor, Q705 removes +5 Vdc from U704 to reset the EEPROM. See the voltage regulator description below.

The EEPROM can be conveniently programmed without any need for opening up the radio. This is accomplished through the microphone jack (J725). The serial data is routed through the Control Board to the EEPROM on the Logic Board.

For an optional 128 channel radio, U704 is replaced with a larger memory (2048 x 8-bit) EEPROM device (19A705553P1).

LATCH

Latch U702 is a CMOS, 3-state, non-inverting, D type flip-flop with the following functions.

- To activate the band switch on the RF Board (if used).

- To function as a digital-to-analog converter (DAC) by generating sine wave signalling tones using resistor network R704.

- To activate the FAST SQUELCH on the Audio Board.

- To activate the low pass filter bypass on the Audio Board when Type 99 tone signalling is used.

RELAY

The relay circuit consists of NPN buffer transistor Q701 and NPN relay driver transistor Q702. The relay is activated by the microprocessor when a Type 99 call is received, or when the public address option is enabled and the mic PTT is keyed. The circuit is capable of handling up to 150 milliamperes from an externally connected relay coil.

VOLTAGE REGULATOR

Voltage regulator U705 supplies a regulated +5 VDC to the microprocessor, the EPROM, the EEPROM and the latch circuit. A reset circuit is built into U705 to provide the microprocessor with a reset signal required during its power-up routine. A +8 volts regulated DC is supplied to regulator U705 from the 8 volt regulator U102, located on the RF Board.

BATTERY VOLTAGE FILTER

Transistor Q703 is a filter circuit for the switched A+ battery voltage. This circuit is used to reduce "alternator whine" interference. SW A+ filtered (13 volts) is used on the Audio Board.

SERVICE NOTES

If a faulty Logic Board is suspected it may be useful to confirm this by substitution of a known good board.

DC CHECKS

Power for the Logic Board is supplied by the 8 volts on J702, Pin 3. This comes from the transmitter regulator U102.

1. Check for +5 volts ±0.25 volts on U705, Pin 5.

2. Check Power-On Reset on U701, Pin 9 (see Figure 2). If not present, check regulator U705, Pin 2 and transistor Q704.
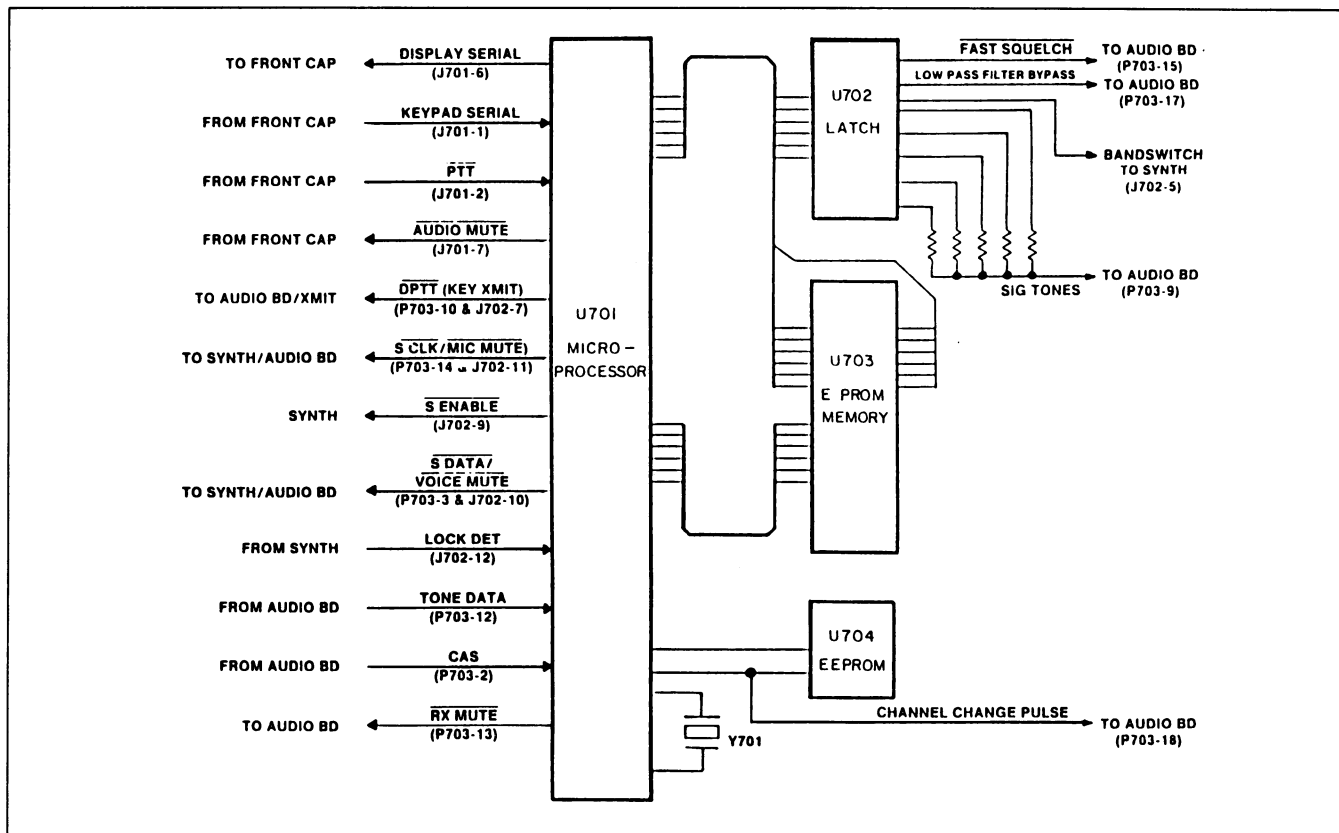
Figure 1 - Block Diagram
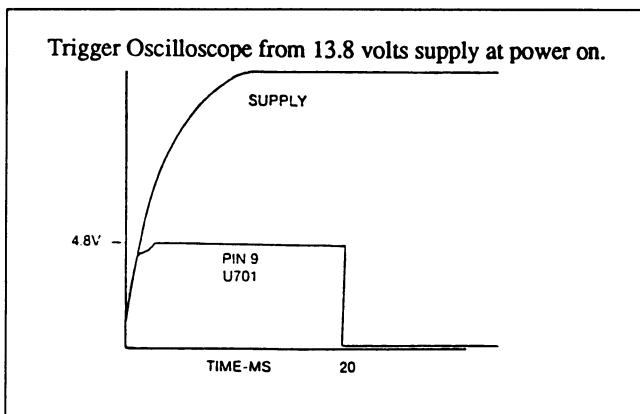
Figure 2 - Reset Waveform
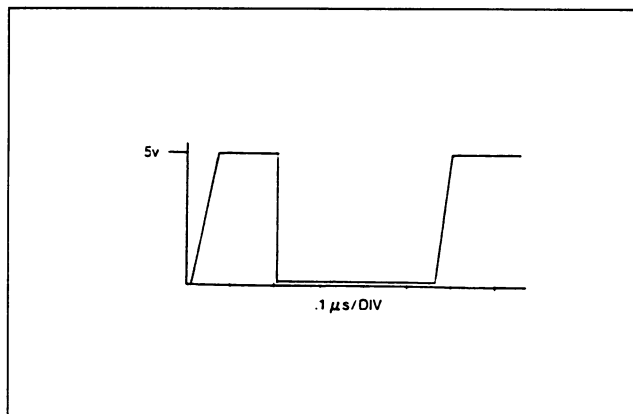
Figure 3 - Ale Clock

3. Check for oscillator activity by examining the ALE-clock on U701, Pin 30 (see Figure 3). If not present, examine the system clock on U701, Pin 18 (5 volts pp at 11.059 MHz). The presence of the system clock, but no ALE may indicate a bad U701. If the system clock is not present, suspect Y701 and related components.

4. All output lines from the microprocessor are pulled high to +5 volts through 50K ohm resistors inside the microprocessor. If a line is high, you may ground that pin and monitor the results. However, if a line is low, the line may not be forced to +5 volts.

EPROM (U703)

SEE PART LIST

PIN CONFIGURATION

V_PP	1		28	V_CC
A_12	2		27	$\overline{PGM}$
A_7	3		26	N C
A_6	4		25	A_8
A_5	5		24	A_9
A_4	6		23	A_11
A_3	7		22	$\overline{CE}$
A_2	8		21	A_10
A_1	9		20	$\overline{CE}$ ALE/$\overline{CS}$
A_0	10		19	O_7
O_0	11		18	O_6
O_1	12		17	O_5
O_2	13		16	O_4
GND	14		15	O_3

FUNCTION DIAGRAM

DATA OUTPUTS
$O_0 - O_7$

$\overline{OE}$

$\overline{PGM}$

CE ALE/$\overline{CS}$

OUTPUT ENABLE
PROG LOGIC
CHIP ENABLE
ADDRESS LATCH ENABLE

OUTPUT BUFFERS

Y DECODE

X DECODE

Y GATING

65,536 BIT
CELL MATRIX

$A_0 - A_{12}$
ADDRESS
INPUTS

$A_0 - A_7$ LATCH
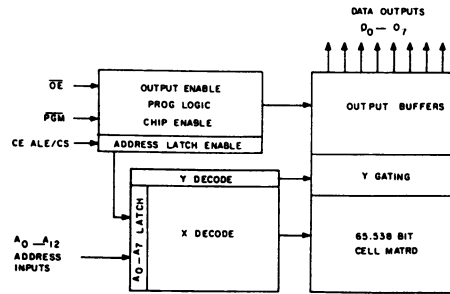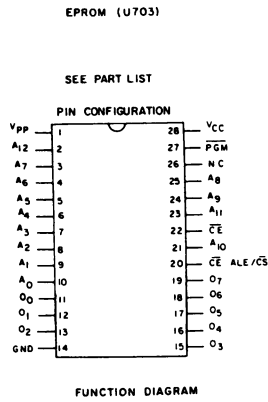
VOLTAGE REGULATOR
(WITH RESET)
19A704970P1
PIN CONFIGURATION

5	+ V_OUT
4	DELAY CAPACITOR (Cd)
3	GROUND
2	RESET OUTPUT
1	+ V_IN

(TAB CONNECTED TO PIN 3)

PNP OUTPUT
TRANSISTOR

INPUT
1

OUTPUT
5

ERROR
AMP

OUTPUT
CURRENT
LIMITER

START

REF

THERMAL
PROTECT

RESET
CIRCUIT

RESET
OUTPUT
2

GROUND
3

3

4 DELAY
CAPACITOR
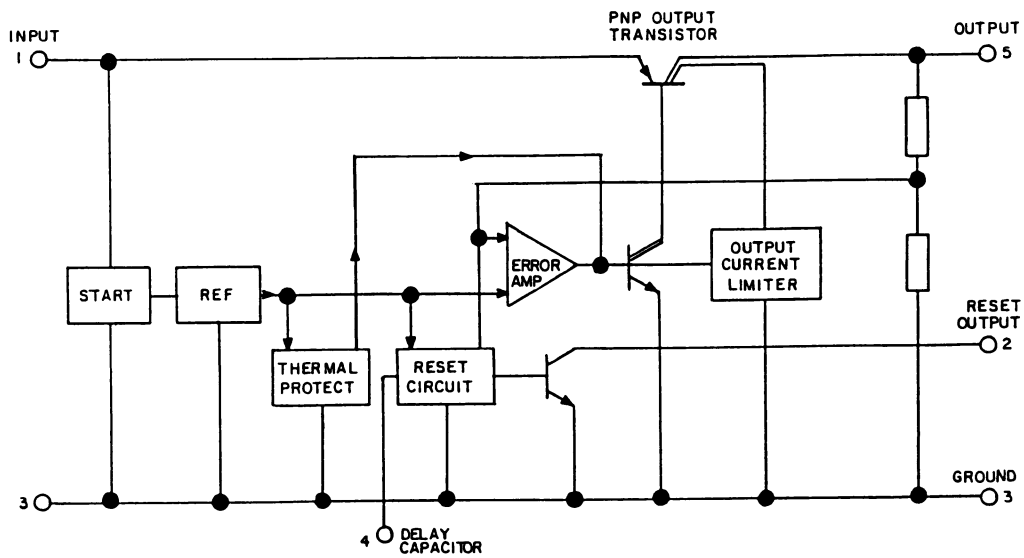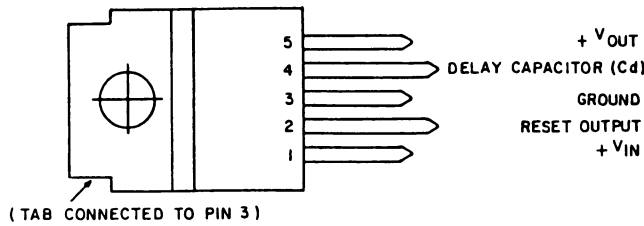
HMOS 8-BIT MICROPROCESSOR (U701)
19A703714P1

PIN CONFIGURATION

```
T2/PI.0   [ 1       40 ]  VCC
T2E2/PI.0 [ 2       39 ]  PO.0
PI.2      [ 3       38 ]  PO.I
PI.3      [ 4       37 ]  PO.2
PI.4      [ 5       36 ]  PO.3
PI.5      [ 6       35 ]  PO.4
PI.6      [ 7       34 ]  PO.5
PI.7      [ 8       33 ]  PO.6
VPD/RST   [ 9       32 ]  PO.7
P3.0/RXD  [ 10      31 ]  EX
P3.I/TXD  [ 11      30 ]  ALE
P3.2/INT0 [ 12      29 ]  PSEN
P3.3/INTI [ 13      28 ]  P2.7
P3.4/T0   [ 14      27 ]  P2.6
P3.5/TI   [ 15      26 ]  P2.5
P3.6/WR   [ 16      25 ]  P2.4
P3.7/RD   [ 17      24 ]  P2.3
XTAL 2    [ 18      23 ]  P2.2
XTAL I    [ 19      22 ]  P2.I
VSS       [ 20      21 ]  P2.0
```
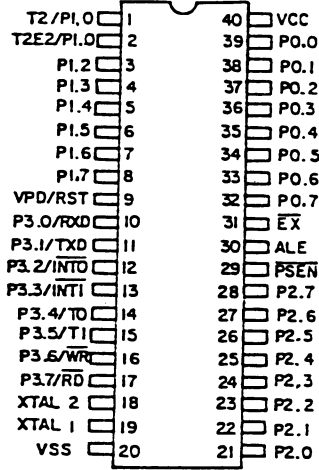
LOGIC SYMBOL
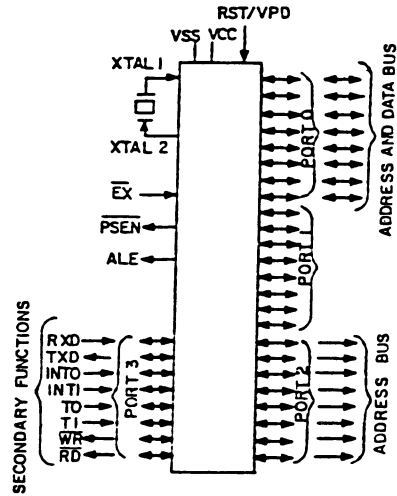
FUNCTION DIAGRAM

LOGIC
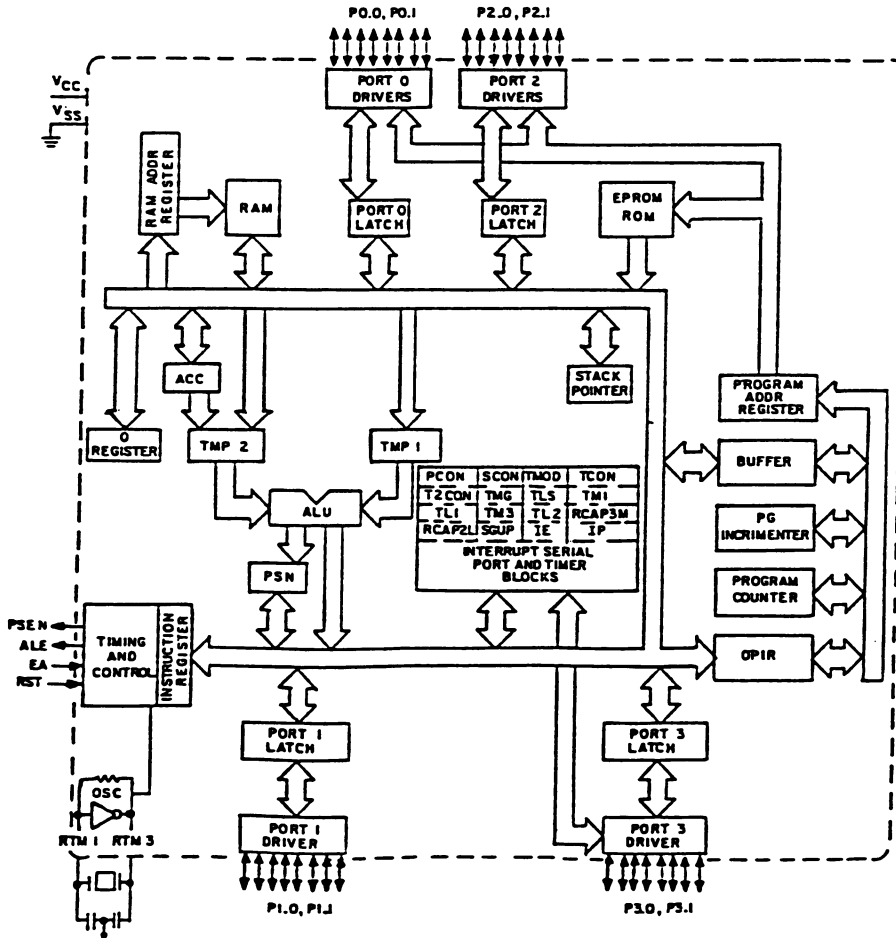
OCTAL 3-STATE D FLIP FLOP (U702)
19A704380P12 (74HC374)

PIN CONFIGURATION

INDENT

PIN "1" LOCATOR

20 19 18 17 16 15 14 13 12 11

TOP VIEW

1 2 3 4 5 6 7 8 9 10

FUNCTION DIAGRAM

TL/F/5336-1
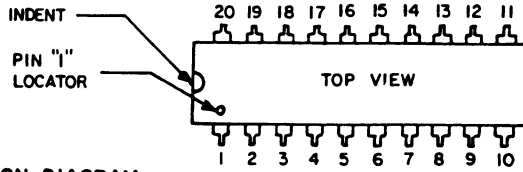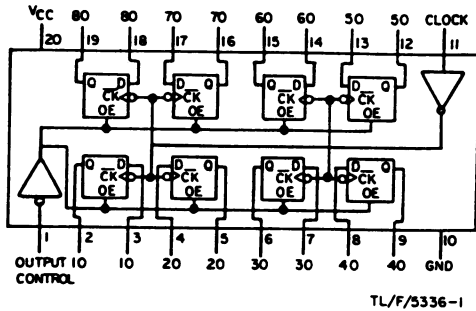
OUTPUT CONTROL

TRUTH TABLE

OUTPUT CONTROL	CLOCK	DATA	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH LEVEL, L = LOW LEVEL
X = DON'T CARE
↑ = TRANSITION FROM LOW-TO-HIGH
Z = HIGH IMPEDANCE STATE
Q_0 = THE LEVEL OF THE OUTPUT BEFORE STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

DIGITAL 512 X 8 EEPROM
19A704724P1
(U704)

PIN CONFIGURATION

A_0 1   X2404   8 V_{CC}
A_1 2   7   TEST
A_2 3   6   SCL
V_{SS} 4   5   SDA
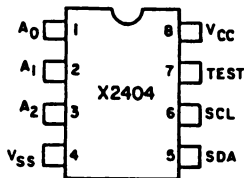
1 A_0 → TO V_{SS}
2 AND 3 A AND A ADDRESS INPUTS
4 V_{SS}
5 SDA SERIAL DATA — I^2C BUS
6 SCL SERIAL CLOCK —
7 TEST INPUT — TO V_{SS}
8 V_{CC}

FUNCTION DIAGRAM

(8) V_{CC} —
(4) V_{SS} —

(5) SDA —

(6) SCL —

(1) A_0
(2) A_1
(3) A_2

START CYCLE

HV GENERATION TIMING & CONTROL

START STOP LOGIC

CONTROL LOGIC

SLAVE ADDRESS REGISTER COMPARATOR

XDEC 64

EEPROM 64X64

WORD ADDRESS COUNTER

LOAD INC

R/$\overline{W}$

YDEC

PIN

CL

DATA REGISTER

D_{OUT} ACR

D_{OUT}
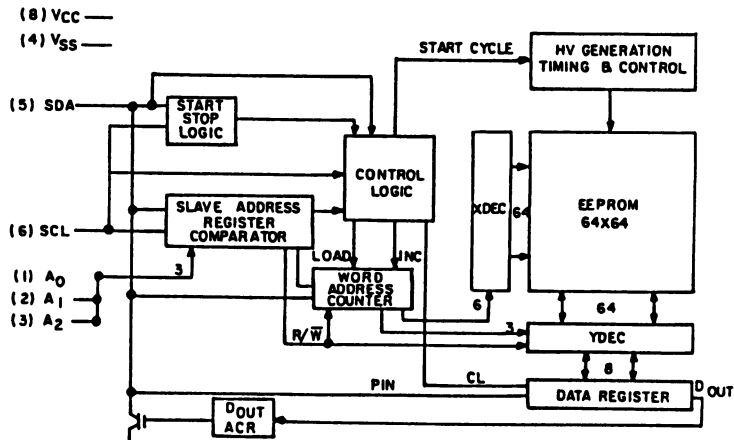
19D901690G5

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C701	19A700121P106	Ceramic: 0.1 µF ±20%, 50 VDCW.
C703	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C704	19A700121P106	Ceramic: 0.1 µF ±20%, 50 VDCW.
C705	19A700235P13	Ceramic: 10 pF ±5%, 50 VDCW.
C706	19A700235P16	Ceramic: 18 pF ±5%, 50 VDCW.
C707	19A704879P2	Electrolytic: 47 µF ±20%, 16 VDCW.
C708	T644ACP410K	Polyester: 0.1 µF ±10%, 50 VDCW.
C709	19A701534P9	Tantalum: 47 µF ±20%, 6.3 VDCW.
C710	19A700121P106	Ceramic: 0.1 µF ±20%, 50 VDCW.
C711 and C712	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, ±30 PPM.
C713 thru C717	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C718 thru C720	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ± 30 PPM.
C721 thru C723	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C725	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C727 and C728	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
		- - - - - - - - - - DIODES - - - - - - - - - -
D701 thru D710	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
		- - - - - - - - - - JACKS - - - - - - - - - - -
J701	19B209727P40	Connector, Plug; sim to AMP 750077-1.
J702	19A704779P11	Connector; sim to Molex 22-17-2122.
		- - - - - - - - - - PLUGS - - - - - - - - - - -
P703	19A704874P1	Connector: sim to: Elco 00-9021-18-12-00-339.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q701	19A700023P2	Silicon, NPN: sim to 2N3904.
Q702 and Q703	19A702503P2	Silicon, NPN: sim to 2N4401.
Q704	19A700023P2	Silicon, NPN: sim to 2N3904.
Q705	19A700022P2	Silicon, PNP: sim to 2N3906.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R701	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R702	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R703	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R704	19A704885P5	Resistive Network: ±2%, 1/8 w.
R705	H212CRP056C	Deposited carbon: 56 ohms ±5%, 1/4 w.
R706	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R707	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.

SYMBOL	PART NO.	DESCRIPTION
R708 thru R711	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R712	H212CRP047C	Deposited carbon: 47 ohms ±5%, 1/4 w.
R713	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R714	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 w.
R715 and R716	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R717 and R718	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
		- - - - - - INTEGRATED CIRCUITS - - - - - - -
U701	19A703714P1	Digital: HMOS 8-bit Microcomputer; sim to TP8032AH.
U702	19A704380P12	Digital: CMOS Octal Tri-State Data Flip-Flop; sim to 74HC374.
U703	19A705561G4	Programmable Memory.
U704	19A704724P1	Digital: 512 x 8 EEPROM (serial I/O); sim to XICOR X2404P.
U705	19A704970P1	Linear: 5 Volt Regulator with Reset Output; sim to SGS L387.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU703	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
XU704	19A700156P15	Socket, IC: 8 Pins, Tin Plated.
		- - - - - - - - - - CRYSTALS - - - - - - - - -
Y701		Quartz: 11.059200 MHz. 19A702511G15

LOGIC

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the description of parts affected by these revisions.

REV. A - LOGIC BOARD 19D901690G5
   To improve operation of the microprocessor changed C711, C712, C719 and C720 and added C718, C726, C727 and C728. Old part numbers were:

   C711 - 19A702052P3, Ceramic: 470 pF ±10%, 50 VDCW.
   C712 - 19A702052P3, Ceramic: 470 pF ±10%, 50 VDCW.
   C719 - 19A702052P3, Ceramic: 470 pF ±10%, 50 VDCW.
   C720 - 19A702052P3, Ceramic: 470 pF ±10%, 50 VDCW.

REV. B - LOGIC BOARD 19D901690G5
   To allow the use of masked parts in m,anufacturing changed R702. Old part number ws:

   R702 - H212CRP310C. Deposited Carbon: 10K ohms ±5%, 1/4 w.

REV. C - LOGIC BOARD 19D901690G5
   To improve operation of the microprocessor added R717 and R718.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

TOP VIEW
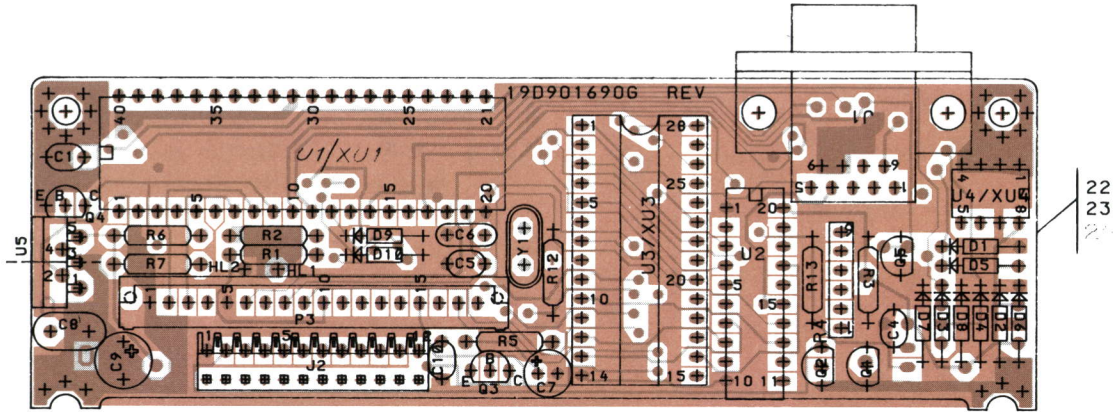
19A705378, Sh. 1, Rev. 0
19A705378, Sh. 2, Rev. 0

SECOND LAYER

FIRST LAYER
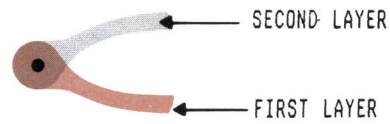
BOTTOM VIEW
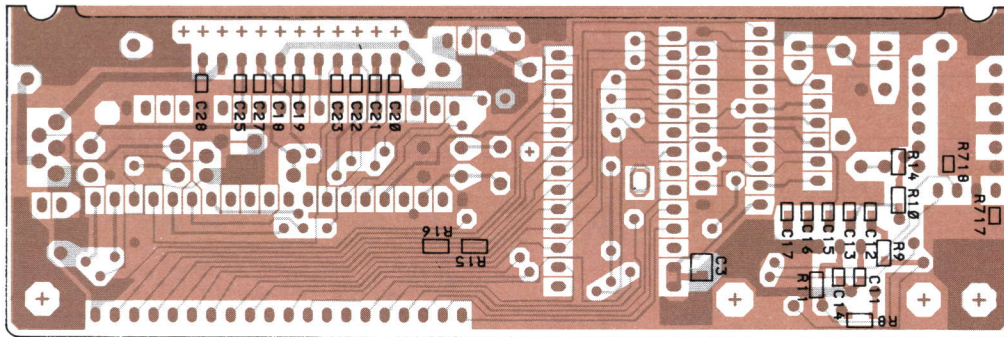
VIEW FROM BACK OF BOARD

19A705378, Sh. 3, Rev. 0
19A705378, Sh. 4, Rev. 0

THIRD LAYER

FOURTH LAYER
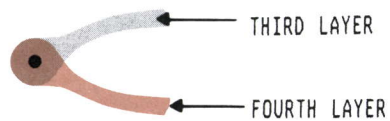
SYSTEM LOGIC BOARD

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
**ELECTROSTATIC
SENSITIVE
DEVICES**

J701

A- 8

DISPLAY SERIAL 6

KEYPAD SERIAL 1

PTT 2

AUDIO MUTE 7

SW A+ FILTERED 3

MIC HI 4
RX AUDIO 5
MIC LO 9

J702

SW A+ 6
A- 1
OPTT 7
LOCK DET 12
S CLK/MIC MUTE 11
S DATA/VOICE MUTE 10
S ENABLE 9
VOL-SQ HI 4
TX MOD 8

P703

S DATA/VOICE MUTE 3
TONE DATA 12
CAS 2
SW A+ FILTERED 16
RX MUTE 13
S CLK/MIC MUTE 14
MIC LO 5
RX AUDIO 6
MIC HI 8
TX MOD 11
VOL-SQ HI 7
OPTT 10
A- 1
SPARE 4

#C711 470P
#C712 470P
#C713 .001u
#C714 .001u
#C715 .001u
#C716 .001u
#C717 .001u

#R708 1k 1/8W
#R709 1k 1/8W
#R710 1k 1/8W
#R711 1k 1/8W

D707
D708
D701
D702
D703
D704
D705
D706

R702 470
HL1 31
HL2

5V

R712 47
Q703
R705 56
C707 47u
C710 .1u

#C718 470P

R701 1k

5V

D709
D710

#C719 470P
#C720 470P
#C721 470P
#C722 470P
#C723 470P

#C725 470P

Y701

R715 100K
R716 100K
C705 10P
C706 10P

U701 uP

U702 LATCH

160k 80k 40k 20k 10k
R704

U703/XU703 EPROM MEMORY

C701 .1u

#C703 .1u

C704 .1u

U704 XU704 E PER. PROM

R706 4.7k
R707 47k
C709 47u
Q704

#R714 2.2k 1/8W
Q705

#R717 10K

R713 4.7k

#R710 10K

5V

PART OF P703

15 FAST SQ
17 LP FILTER BYPASS
18 CHANNEL CHANGE PULSE
9 SIG TONES

R703 1k
Q701 Q702

PART OF J702

2 RELAY
#C726 470P

5 BAND SWITCH
#C727 470P

U705 5V REG

3 +8V

C708 .1u

NOTES:
1. ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER u,n, OR P.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR u.

2. CUT RUN BETWEEN HL1 AND HL2 WHEN MASKED MICROPROCESSOR IS INCORPORATED.

3. #IDENTIFIES CHIP COMPONENTS WHICH ARE LOCATED ON SOLDER SIDE OF PWB.

MODEL NO.	REV. LETTER
PL19D901690G5	C

PWR AND GND CONNECTIONS

DEVICE	VCC PIN NO.	GND PIN NO.
U701	40	20
U702	20	10
U703	1,27,28	14
U704		1,2,3,4

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

(19D902179, Sh. 3, Rev. 5)

SYSTEM LOGIC BOARD