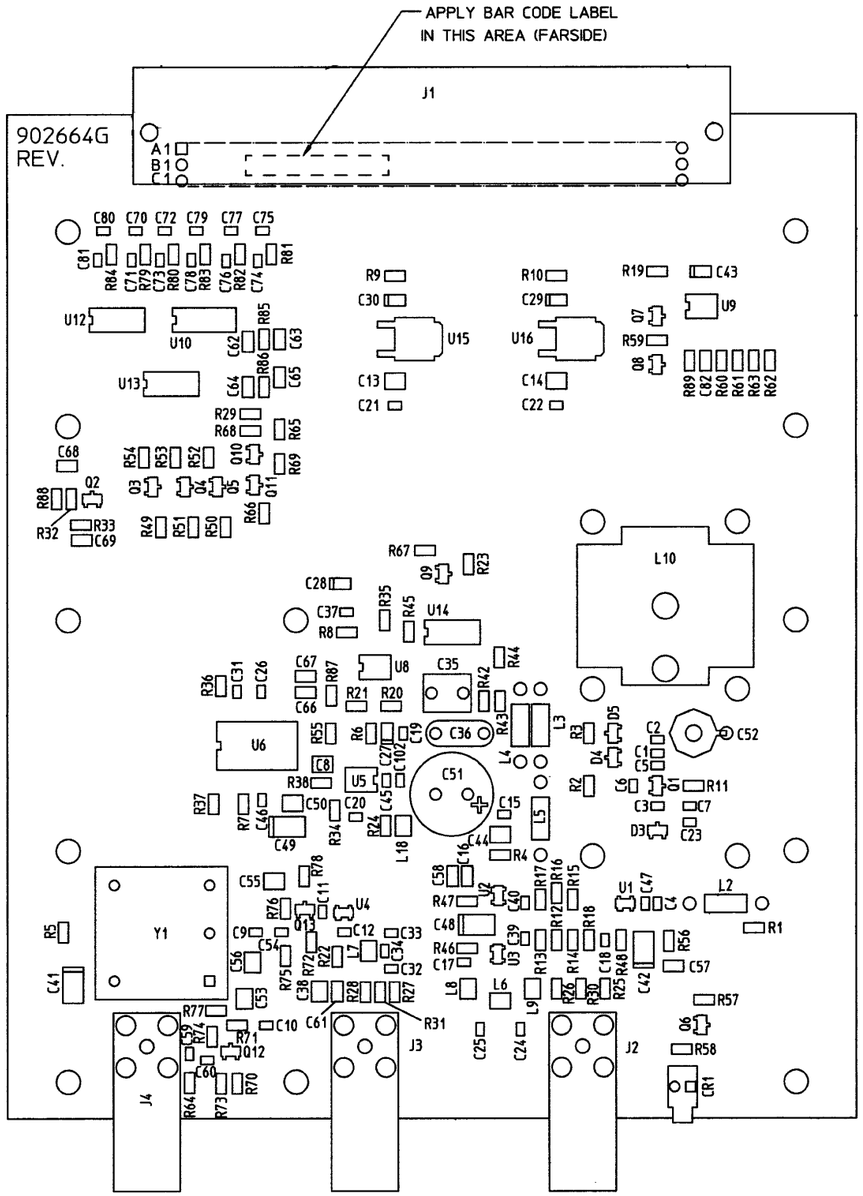
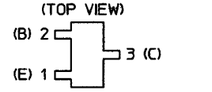
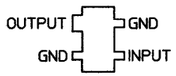


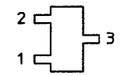
LEAD IDENTIFICATION FOR
Q1-Q8
(SOT) TRANSISTORS
(TOP VIEW)

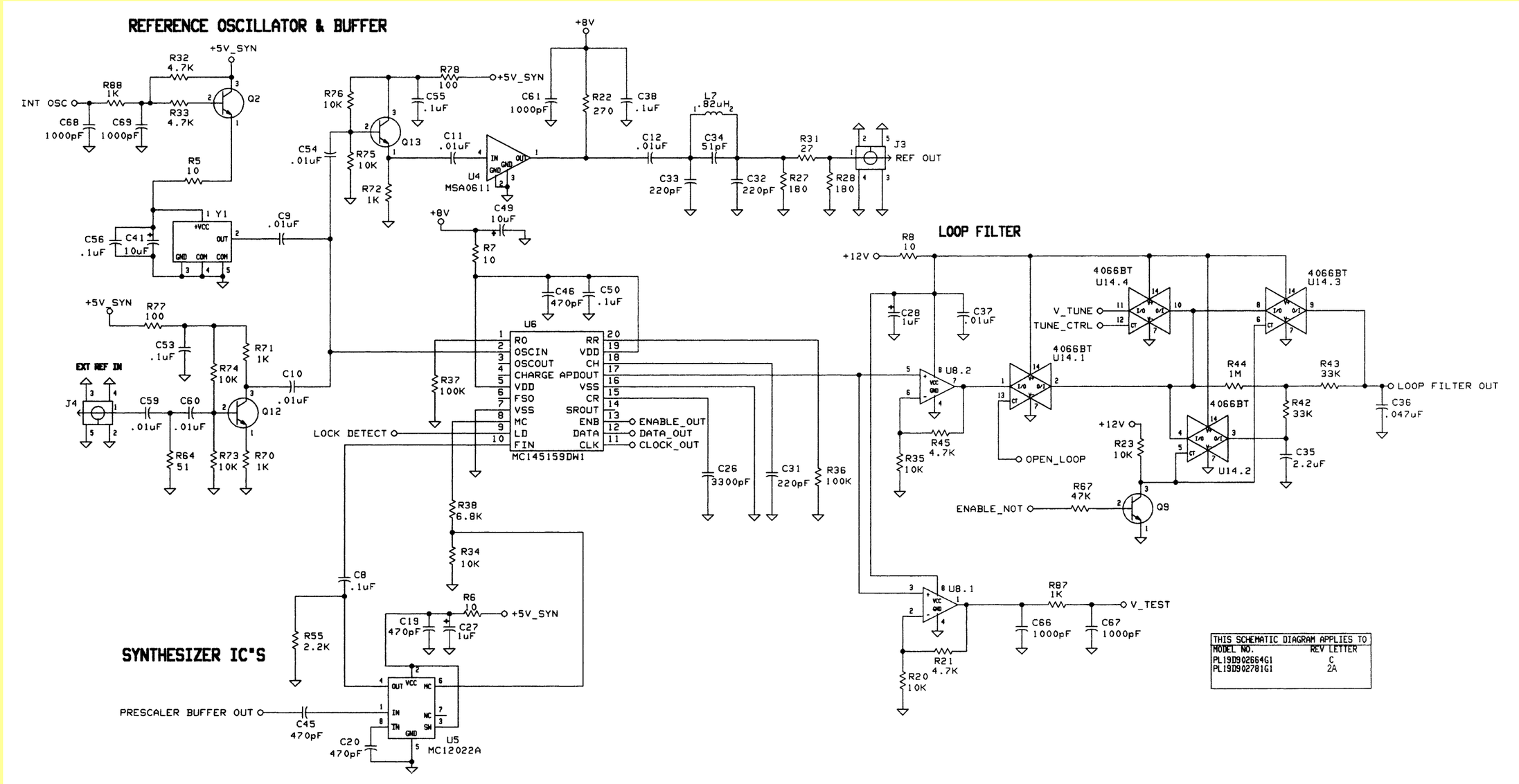


LEAD IDENTIFICATION FOR
U1-U4
(SOT) INT CKT
(TOP VIEW)

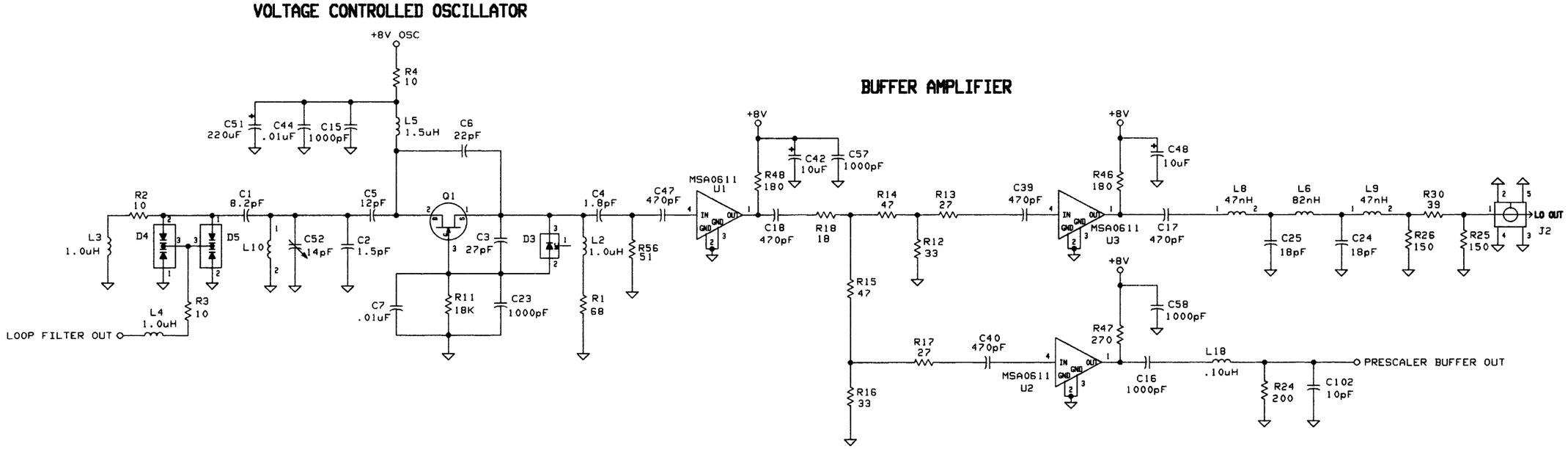


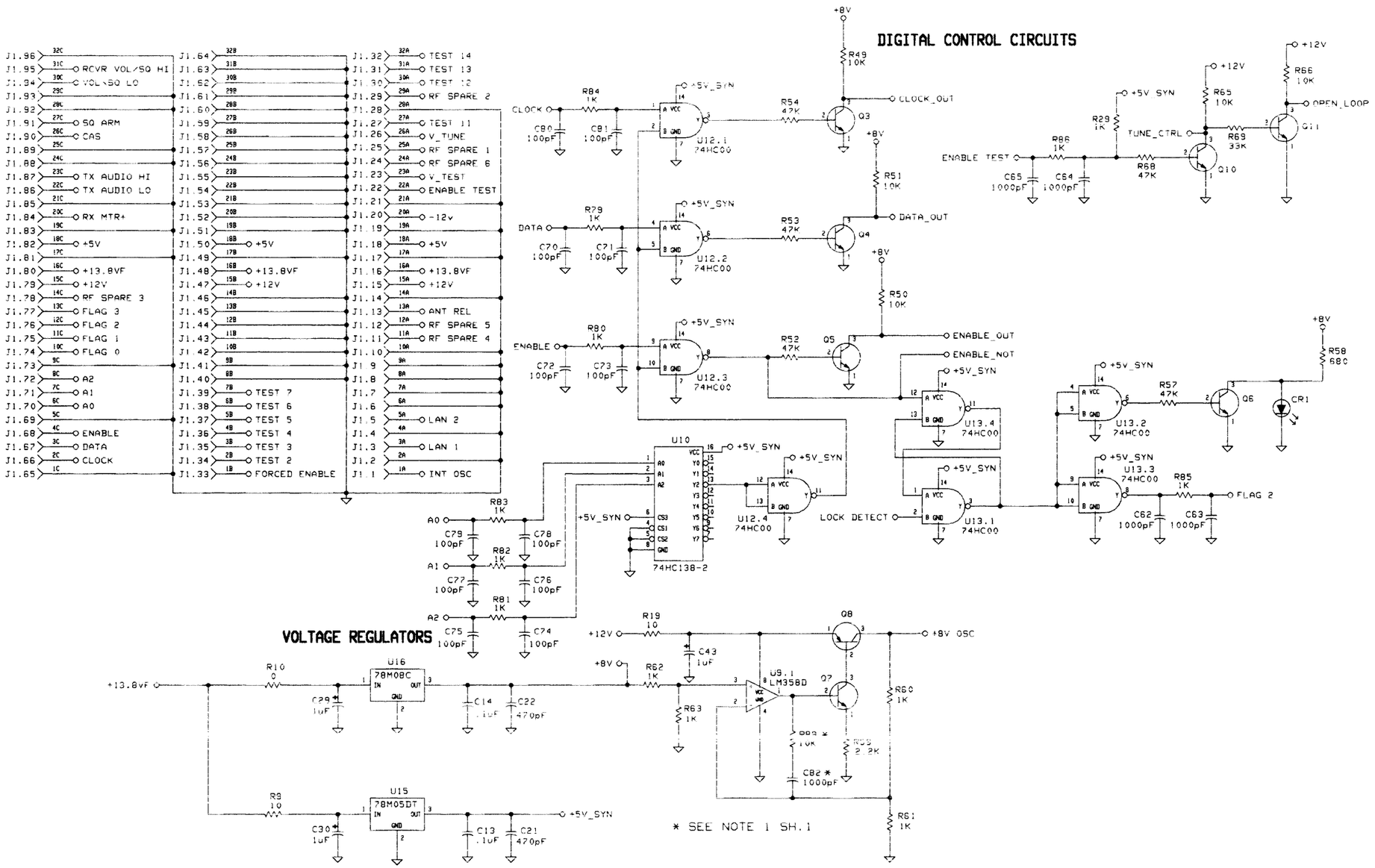
LEAD IDENTIFICATION FOR
D3-D5
(SOT) DIODES
(TOP VIEW)



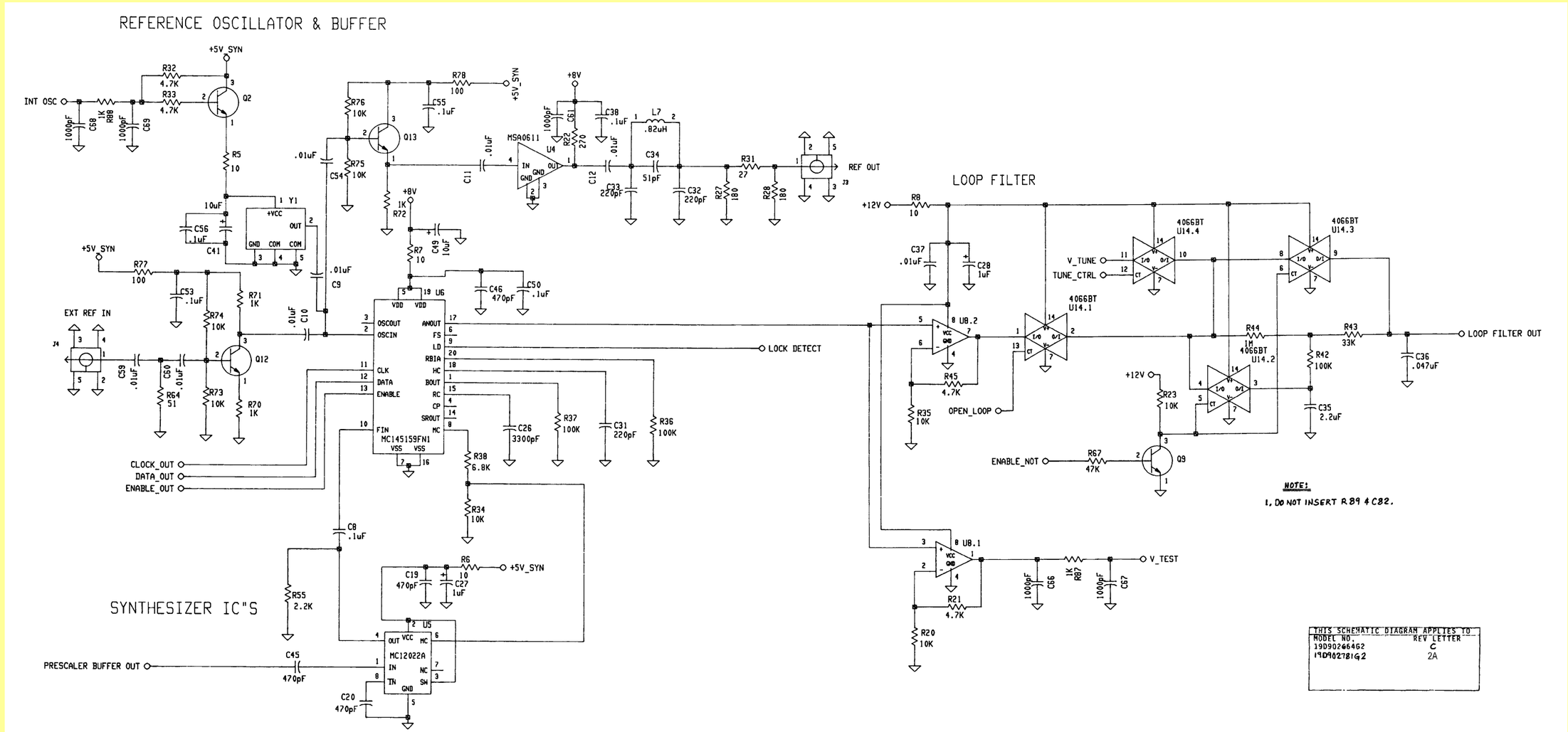


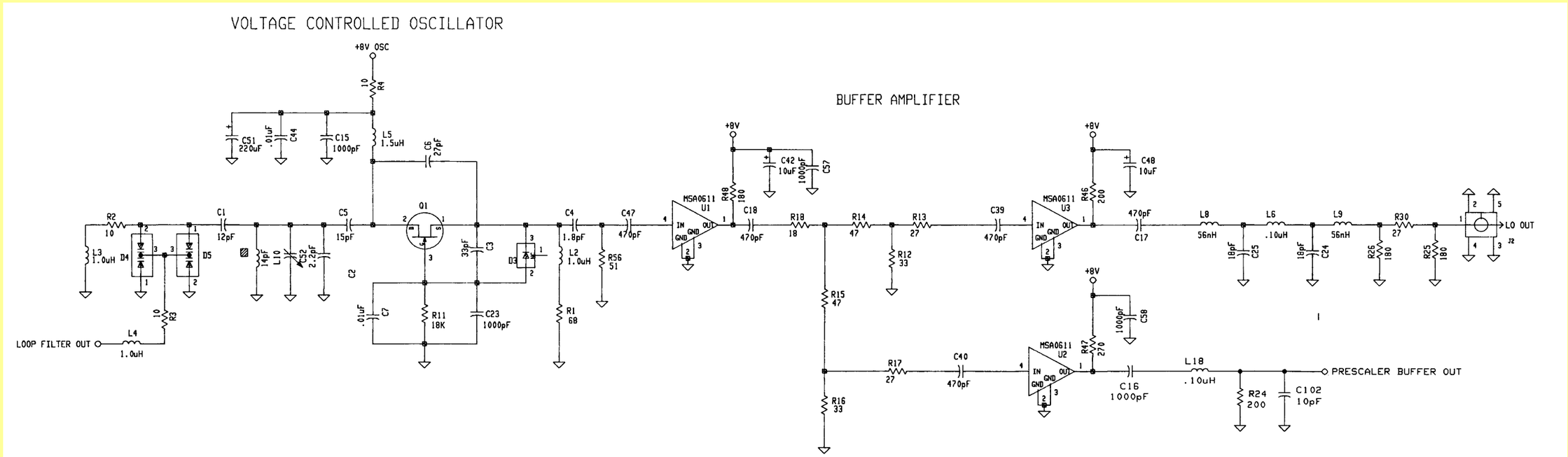
VHF RECEIVER SYNTHESIZER MODULE 19D902781G1
(19D903621, Sh. 1, Rev. 5)


VOLTAGE CONTROLLED OSCILLATOR
+8V OSC
R4 10
C51 220uF
C44 .01uF
C15 1000pF
L5 1.5uH
C6 22pF
R2 10
C1 8.2pF
C5 12pF
Q1
C4 1.8pF
C47 470pF
L3 1.0uH
D4
D5
L10
C52 14pF
C2 1.5pF
C3 27pF
D3
L2 1.0uH
R56 51
L4 1.0uH
R3 10
LOOP FILTER OUT
C7 .01uF
R11 18K
C23 1000pF
R1 68
BUFFER AMPLIFIER
MSA0611 U1
+8V
C42 10uF
C57 1000pF
R48 180
C18 470pF
R18 18
R14 47
R13 27
R12 33
R15 47
R16 33
C39 470pF
MSA0611 U3
R46 180
C48 10uF
C17 470pF
L8 47nH
L6 82nH
L9 47nH
R30 39
C25 18pF
C24 18pF
R26 150
R25 150
J2
LO OUT
C58 1000pF
R47 270
R17 27
C40 470pF
MSA0611 U2
C16 1000pF
L18 .10uH
R24 200
C102 10pF
PRESCALER BUFFER OUT

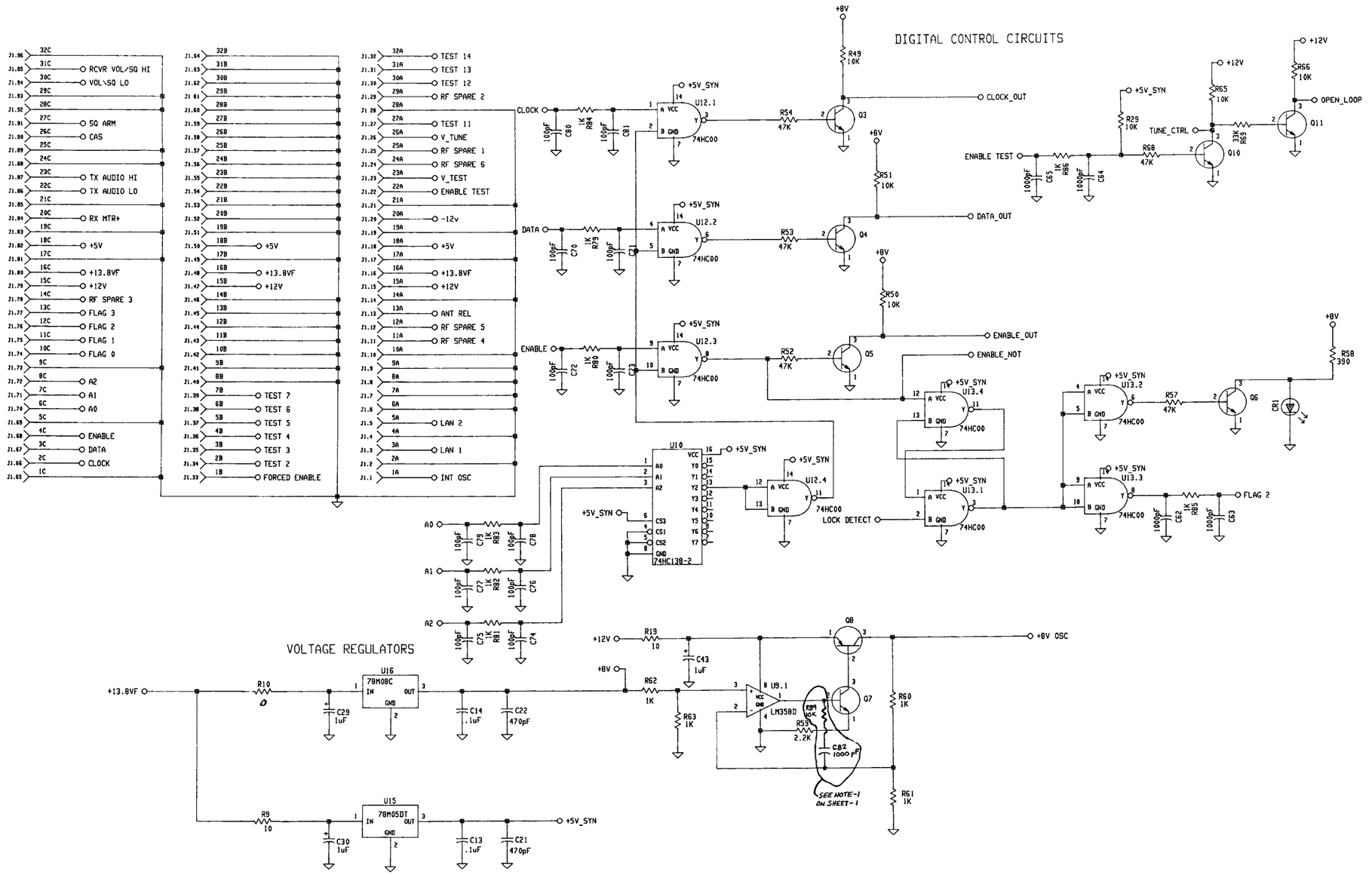


VHF RECEIVER SYNTHESIZER MODULE 19D902781G1
(19D903621, Sh. 3, Rev. 5)


REFERENCE OSCILLATOR & BUFFER
SYNTHESIZER IC"S
LOOP FILTER
INT OSC
EXT REF IN
CLOCK_OUT
DATA_OUT
ENABLE_OUT
PRESCALER BUFFER OUT
LOCK DETECT
REF OUT
LOOP FILTER OUT
V_TUNE
TUNE_CTRL
OPEN_LOOP
ENABLE_NOT
V_TEST
MC145159FN1
MC12022A
MSA0611
4066BT
NOTE:
1. DO NOT INSERT R89 & C82.
THIS SCHEMATIC DIAGRAM APPLIES TO
MODEL NO. REV LETTER
19D902664G2 C
19D902781G2 2A



VHF RECEIVER SYNTHESIZER MODULE 19D902781G2
(19D903769, Sh. 2, Rev. 4)


DIGITAL CONTROL CIRCUITS
32C
31C RCVR VOL/SQ HI
30C VOL\SQ LO
29C
28C
27C SQ ARM
26C CAS
25C
24C
23C TX AUDIO HI
22C TX AUDIO LO
21C
20C RX MTR+
19C
18C +5V
17C
16C +13.8VF
15C +12V
14C RF SPARE 3
13C FLAG 3
12C FLAG 2
11C FLAG 1
10C FLAG 0
9C
8C A2
7C A1
6C A0
5C
4C ENABLE
3C DATA
2C CLOCK
1C
32B
31B
30B
29B
28B
27B
26B
25B
24B
23B
22B
21B
20B
19B
18B +5V
17B
16B +13.8VF
15B +12V
14B
13B
12B
11B
10B
9B
8B
7B TEST 7
6B TEST 6
5B TEST 5
4B TEST 4
3B TEST 3
2B TEST 2
1B FORCED ENABLE
32A TEST 14
31A TEST 13
30A TEST 12
29A RF SPARE 2
28A
27A TEST 11
26A V_TUNE
25A RF SPARE 1
24A RF SPARE 6
23A V_TEST
22A ENABLE TEST
21A
20A -12v
19A
18A +5V
17A
16A +13.8VF
15A +12V
14A
13A ANT REL
12A RF SPARE 5
11A RF SPARE 4
10A
9A
8A
7A
6A
5A LAN 2
4A
3A LAN 1
2A
1A INT OSC
CLOCK
DATA
ENABLE
+8V
+5V_SYN
+12V
R49 10K
R54 47K
Q3
CLOCK_OUT
U12.1
74HC00
R51 10K
R53 47K
Q4
DATA_OUT
U12.2
R50 10K
R52 47K
Q5
ENABLE_OUT
ENABLE_NOT
U12.3
U13.4
U13.2
U13.1
U13.3
U12.4
R57 47K
Q6
CR1
R58 390
R56 10K
OPEN_LOOP
Q11
R65 10K
TUNE_CTRL
Q10
R29 10K
R68 47K
ENABLE TEST
FLAG 2
LOCK DETECT
U10
74HC138-2
A0
A1
A2
VOLTAGE REGULATORS
U16
78M08C
U15
78M05DT
R10 0
R9 10
C29 1uF
C30 1uF
C14 .1uF
C13 .1uF
C22 470pF
C21 470pF
R19 10
R62 1K
R63 1K
C43 1uF
U9.1
LM358D
R59 2.2K
C82 1000 pF
Q8
Q7
R60 1K
R61 1K
+8V OSC
SEE NOTE-1 ON SHEET-1

ADDENDUM NUMBER 1 TO MAINTENANCE MANUAL
LBI-38641F
Refer to ECO#20026373

GENERAL

The addendum identifies production changes to the MASTR® III VHF Receiver Synthesizer Module 19D902781G1 & G2. New diagrams are also included.

PRODUCTION CHANGE

Rev. 2A **Receiver Synthesizer Module 19D902780G1 & G2**

To reduce RF emissions, the conductive connector grommet was replaced with a thicker part to ensure contact with the front panel at RF connectors. RF Sheilding Grommet was changed from 19B802690P1 to 19D802690P2.

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Printed in U.S.A.

VHF RECEIVER SYNTHESIZER MODULE
19D902781G1 & G2

TABLE OF CONTENTS

DESCRIPTION

The Receiver Synthesizer Module provides the local oscillator signal (LO) to the Receiver Front End Module of the MASTR III base station. The module also provides the reference oscillator signal to the transmitter synthesizer. Receiver Synthesizer Module 19D902781G1 (Group 1) generates an output injection signal in the 157 to 172 MHz range, and 19D902781G2 (Group 2) generates a signal in the 129 to 152 MHz Range.

The Receiver Synthesizer Module is a phase-locked loop (PLL) design, as shown in the block diagram (Figure 1). Its output is generated directly by the VCO Q1 and buffered by Monolithic Microwave Integrated Circuits (MMIC) U1 and U3.

The logic signals from controller (U10, 12, and 13) determine the synthesizer frequency. Frequency stability is maintained by either using the internal reference oscillator Y1 or by applying a high precision reference signal to the EXT Reference Oscillator Port J4. The internal reference oscillator is a temperature controlled crystal oscillator (TCXO) operating at 12.8 MHz. The oscillator has a stability of ±1.5 ppm over the temperature range of -30°C to +75°C. See the table containing General Specifications for the minimum external oscillator specifications.

The buffered VCO output is sampled by the resistive splitter and conditioned by buffer amplifier U2. It is then fed to the divide by 64/65 dual modulus prescaler U5. The divided output from the prescaler is connected to the F_{in} input of the PLL U6. Within the PLL the divided VCO input signal F_{in} is divided again. The PLL also divides down the 12.8 MHz reference signal. Three inputs from the controller; ENABLE, CLOCK, and serial DATA program the PLL divider circuits.

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Lynchburg, Virginia 24501
(Outside USA, 434-385-2400) Toll Free 800-528-7711
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The divided reference signal and the divided VCO signal are compared in the PLL phase detector. When the reference and VCO signals are identical the PLL phase detector generates a constant DC output voltage. This voltage is buffered by U8 and filtered by the loop filter circuit. It is then applied to Q1 setting the VCO on frequency.

If the compared frequencies (phases) differ, an error voltage is generated which adjusts the VCO frequency. During this out-of-lock condition, the PLL also sends a Lock Detect signal (LD) to the controller and lights the FAULT LED on the front panel of the module.

TABLE 1 - GENERAL SPECIFICATIONS

ITEM	SPECIFICATION	
FREQUENCY TUNING	INJECTION FREQ.	FREQ. BAND
Output Injection Signal	157.4 MHz - 172.2 MHz (G1)	136 MHz - 150.8 MHz
	129.4 MHz - 152.6 MHz (G2)	150.8 MHz - 174 MHz
Electrical		
Full Specifications	2 MHz	
Degraded Specifications	3 MHz	
Channel Spacing	5 kHz	
FREQUENCY STABILITY	±1.5 ppm	
LO POWER OUTPUT	1.5 dBm ±1.5 dBm	
LO NOMINAL IMPEDANCE	50 Ohms	
PHASE NOISE		
@ 25 kHz Offset	-142 dBc/Hz	
@ 30 kHz Offset	-147 dBc/Hz	
HUM AND NOISE		
Companion Receiver	-60 dB	
HARMONICS @ LO PORT	<-30 dBc	
SWITCHING SPEED	< 50 ms	
CURRENT DRAIN	<200 mA	
+13.8V	<50 mA	
+12V		
REFERENCE OSCILLATOR		
Frequency Output	12.8 MHz ±1.5 ppm	
Power Output	0 dBm ±1.5 dBm	
Impedance	50 ohms	
EXT. REFERENCE OSCILLATOR		
Frequency Output	5.00 MHz to 17.925 MHz (must be divisible by the channel spacing)	
Power Output	10 dBm ±3 dBm into 50 ohms	
Impedance	50 ohms	

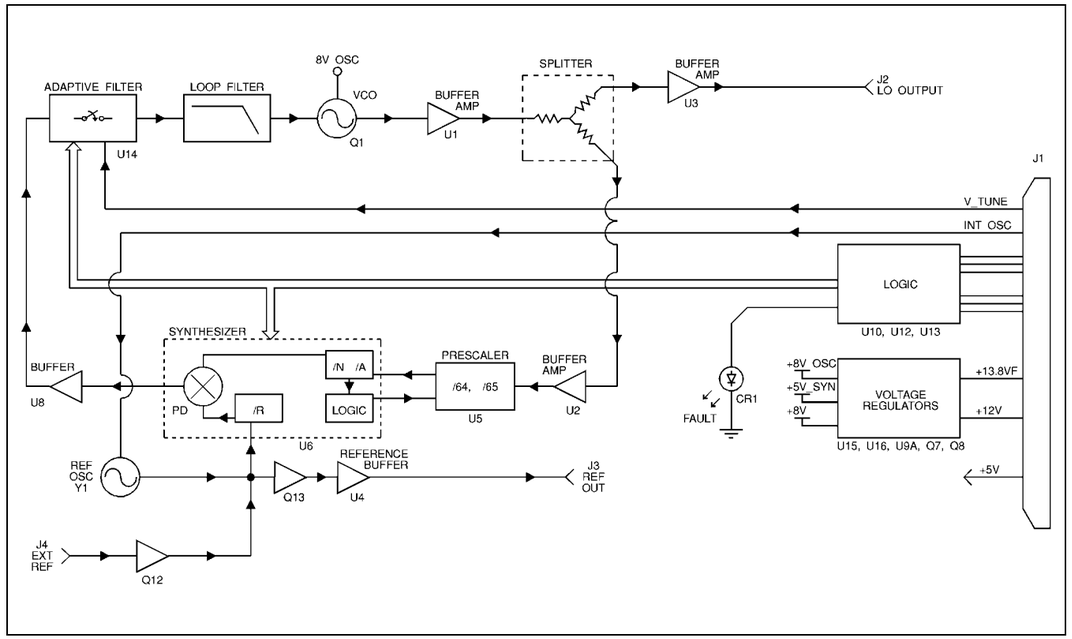


Figure 1 - Receiver Synthesizer Block Diagram

CIRCUIT ANALYSIS

The Receiver Synthesizer Module consists of the following circuits:

- Voltage Controlled Oscillator
- Buffer Amplifiers
- Reference Oscillator and Buffer
- Prescaler and Synthesizer
- Loop Filter
- Digital Control
- Voltage Regulators

VOLTAGE CONTROLLED OSCILLATOR

The free running Voltage Controlled Oscillator (VCO) is composed of a grounded-gate JFET (Q1) and associated circuitry. Inductor L10 and associated capacitors form the resonant tank circuit. The circuit's use of high-Q components minimizes phase noise.

Frequency tuning of the VCO is done by changing the DC output voltage level from the loop filter U14. The Loop Filter Out signal from U14 is routed through L4 and R3 and applied to the two varicap diodes D4 and D5. The voltage level applied determines the diodes' capacitance and sets the resonant frequency of the oscillator. If the VCO drifts or the frequency is changed, the DC voltage level changes causing the VCO's resonant frequency to change. The output of the oscillator is then applied to a buffer amplifier. Course adjustment of frequency is done by adjusting trimmer capacitor C52 while applying a calibration voltage to the V_TUNE line connected to U14.4-11.

BUFFER AMPLIFIERS

The MMIC Buffer Amplifier stage is composed of three MMICs (U1, U2, and U3) and a resistive splitter. The amplifiers serve two purposes; amplifying the local oscillator signal (LO OUTPUT) for injection into the Receiver Front End assembly and providing a feedback signal to the synthesizer Phase-Locked Loop (PLL).

Integrated circuits U1 and U3 provide amplification of the local oscillator signal. The output of U1 is fed to a resistive signal splitter composed of R13 through R18. One of the resistive signal splitter outputs drives amplifier U3. The U3 output signal is coupled by C17 to a low-pass filter network (C24 and C25, L6, L8, and L9) and a resistive pad (R25, R26 and R30) for isolation. The local oscillator signal is finally routed to J2, LO OUT, for connection to the Receiver Front End Assembly. The LO output level at BNC connector J2 is nominally 0 dBm.

The other output of the resistive signal splitter drives U2. The amplified output from U2, PRESCALER BUFFER OUT, is coupled to the 50 ohm input of the prescaler U5 via capacitors C16 and C45.

REFERENCE OSCILLATOR AND BUFFER

The reference oscillator section provides a reference signal to the PLL section. The circuit design allows using either an external or internal oscillator.

When using an external oscillator, the internal oscillator is disabled by placing a logic low on the INT OSC line from the T/R Shelf Interface Board. A high precision external oscillator may then be connected to the module through the external reference oscillator connector J4, EXT REF IN. J4 has a 50 ohm input impedance and is coupled to the base of Q12. Buffer Q12 conditions the signal and applies it to the synthesizer U6 via coupling capacitor C10.

The internal reference oscillator, Y1, provides a 12.8 MHz signal with a stability of ±1.5 ppm. It is enabled by applying a logic high signal on the INT OSC line. This signal turns on Q2, allowing it to conduct and apply +5 volts to pin 1 of the oscillator Y1. The 12.8 MHz output signal (Y1 pin 2) is then sent to the synthesizer via coupling capacitor C9.

The reference oscillator signal, either external or internal, is also routed to Q13 via coupling capacitor C54. The output taken from the emitter of Q13 is applied through C11 to the input of Buffer Amplifier U4. The buffered signal is coupled through C12 to a low pass filter network (C32,C33,C34, and L7) and a resistive pad (R27, R28, and R31) for isolation. The output from the resistive pad is then connected to J3, REF OUT, making the reference oscillator signal available for external use.

PRESCALER AND SYNTHESIZER IC

The integrated circuit U6 is the heart of the synthesizer. It contains the necessary frequency dividers and control circuitry to synthesize output frequencies by the technique of dual modulus prescaling. U6 also contains an analog sample and hold phase detector and a lock detector circuit.

Within the U6 are three programmable dividers which are serially loaded using the CLOCK, DATA, and ENABLE inputs (pins 11, 12, and 13 respectively). A serial data stream (DATA) on pin 12 is shifted into the internal shift registers by low to high transitions on the clock input (CLOCK) at pin 11. A logic high (ENABLE) on pin 13 then transfers the program information from the shift registers to the divider latches. The serial data determines the VCO frequency by setting the internal R, A, and N dividers.

The 12.8 MHz reference oscillator signal OSCIN is internally routed to the "R" divider. The "R" divider divides down the 12.8 MHz reference signal to a lower frequency, F_r, as directed by the input data and applies the signal to the internal analog phase and lock detectors.

The "A" and "N" dividers process the loop feedback signal from the VCO (by way of the dual modulus prescaler U5). The output of the "N" divider, F_v, is a divided down version of the VCO output frequency. This signal is also applied to the internal phase detector. The ramp and hold constants are determined by C26, R37, C31, and R36.

The analog phase detector output voltage (PD OUT) is proportional to the phase difference between F_v and F_r. This output serves as the loop error signal. When operating on the correct frequency, the inputs to the phase detector are identical and the output voltage of the analog phase detector is constant. If the compared frequencies (phases) differ, the analog phase detector increases or decreases the DC output voltage (PD OUT). This error signal voltage tunes the VCO to whatever frequency is required to keep F_v and F_r locked (in phase).

The lock detector furnishes the Fault circuit in U13 with the lock detect (LD) signal. When F_v and F_r are in phase, the lock detector output sends a logic high on the LD line to the fault circuit U13. If the VCO is not locked onto the correct frequency, the resulting out-of-phase condition causes the output from the lock detector to be a logic low.

LOOP FILTER

The error signal, ANOUT, is applied to the loop filter at U8.2-5 and U8.1-3. U8.2 acts as a buffer amplifier with gain. The output signal from the amplifier is applied to a loop filter consisting of R42, R43, R44, C35 and C36 via the bilateral switch U14. The filter removes noise and sampling frequencies from the error voltage. The switch, U14, selects the proper filter configuration for operation in the narrow band, wide band or tuning mode. The control signals (OPEN_LOOP, ENABLE_NOT, and TUNE_CTRL) for U14 are derived from the digital control circuits U10, U12, and U13. U8.1 provides a buffered output for testing at the DIN connector on the rear of the module.

DIGITAL CONTROL

Logic control circuits (other than those inside the synthesizer IC - U6) consist of the following:

- Digital Control Circuit (U10, U12, & U13)
- Level Shifters
- Fault Circuit

The Digital Control Circuits U10, U12, & U13 serve as an interface between the controller and the synthesizer IC.

As an address decoder, U10 enables the input gates when the A0, A1, and A2 input lines (pins 4, 3, and 2) receive the correct address code from the controller. For the Receiver synthesizer the enable address is 010 on A0, A1, and A2 respectively. After receiving the proper logic code, the input gate U12 is enabled. This allows the ENABLE, CLOCK, and serial DATA information to pass on to the synthesizer via the level shifters.

The Level Shifters Q3, Q4, and Q5 convert the five (5) volt logic level to the eight (8) volt logic level required by the synthesizer.

The Fault circuit, U13, monitors the lock detect signal from the PLL synthesizer. Under normal (locked) condition, the PLL sends a logic high signal to U13. U13 processes the signal and providing a logic high output which saturates Q6. With Q6 saturated, the FAULT LED (CR1) turns off. U13 also sends a logic high signal, FLAG 2, (U13.3-8) to the controller indicating the VCO's frequency is correct.

When the VCO is not on the correct frequency, the synthesizer sends a logic low signal to U13. This causes U13 to cutoff Q6 which turns on the FAULT LED. U13 also sends a logic low signal to the controller indicating the VCO's frequency is incorrect.

VOLTAGE REGULATORS

Voltage regulators U15 and U16 reduce the +13.8 VF line to +5 Vdc and +8 Vdc respectively. The output from U15 (+5V_SYN) is used by both the synthesizer and logic circuitry while the 8 Vdc output from U16 is used for the op-amps, level shifters, and the discrete +8V OSC regulator circuit.

The discrete +8V OSC regulator circuit is a linear regulator consisting of U9A, Q7, Q8, and associated circuitry. The error amplifier U9A controls Q7 and pass element Q8. The +8V OSC is used as the power source for the VCO circuit, where additional filtering is provided to keep noise to a minimum

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the Synthesizer Module:

1. Modulation Analyzer; HP 8901A, or equivalent
2. Power Supply; 12.0 Vdc @ 500 mA
3. Frequency Counter; 10 MHz - 250 MHz
4. Power Meter; -20 dBm to +10 dBm
5. Spectrum Analyzer; 0 - 1 GHz

TEST AND ALIGNMENT

Initialization

Apply +12 Vdc to the test fixture.

Current consumption

Measure the current through pins 15A,15B, 15C, 16A, 16B, and 16C.

Verify the current is less than 250 mA. Total current is the +13.8 VF current and +12 Vdc current combined.

Reference Oscillator

Adjust Y1 for an output frequency of 12.8 MHz ±5 Hz. Measure the output power of the reference oscillator output (J3).

Verify the output power is 0 dBm ±1.5 dBm.

Oscillator Alignment

Ground the ENABLE TEST line (pin 22A). Apply +5 Vdc to the V_TUNE line (pin 26A). Measure the frequency of the free running oscillator at the LO OUT port (J2).

SERVICE NOTES

The following service information applies when aligning, testing, or troubleshooting the RX Synthesizer:

- Logic Levels:
  Logic 1 = high = 4.5 to 5.5 Vdc
  Logic 0 = Low = 0 to 0.5 Vdc
- Receiver Synthesizer Address = A0 A1 A2 = 010
- Synthesizer data input stream is as follows:

  14-bit "R" divider most significant bit (MSB) = R13 through "R" divider least significant bit (LSB) = R0

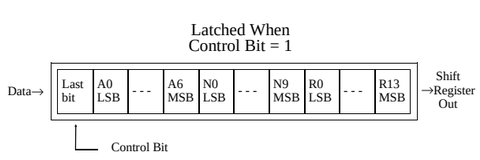
  10-bit "N" divider MSB = N9 through "N" divider LSB = N0

  7-bit "A" divider MSB = A6 through "A" divider LSB = A0

  Single high Control bit (last bit)

  Latched When Control Bit = 1

DATA ENTRY FORMAT



- Synthesizer lock is indicated by the extinguishing of the front panel LED indicator and a logic high on the fault FLAG 2 line (J1 pin 12C).
- Always verify synthesizer lock after each new data loading.

Adjust the trimmer capacitor C52 to the correct frequency:

Group 1 - 170 MHz ±100 kHz.

Group 2 - 150 MHz ±100 kHz.

Synthesizer Loading

Unground the ENABLE TEST line (pin 22A). Load the synthesizer IC Group 1 - 170 MHz.

Group 2 - 150 MHz.

Verify the lock indicator (CR1) is off or the FLAG 2 line is high.

Hum and Noise

Initialize the HP 8901A for 300 Hz - 3 kHz, 750 us deemphasis, average FM deviation, and 0.44 dB reference for the deviation.

Verify the hum and noise (J2) is less than -55 dB.

Output Power and Harmonic Content

Verify the output power (J2) at the fundamental frequency is:

0 dBm ±2.0 dB

Verify the harmonic content is less than -30dBc.

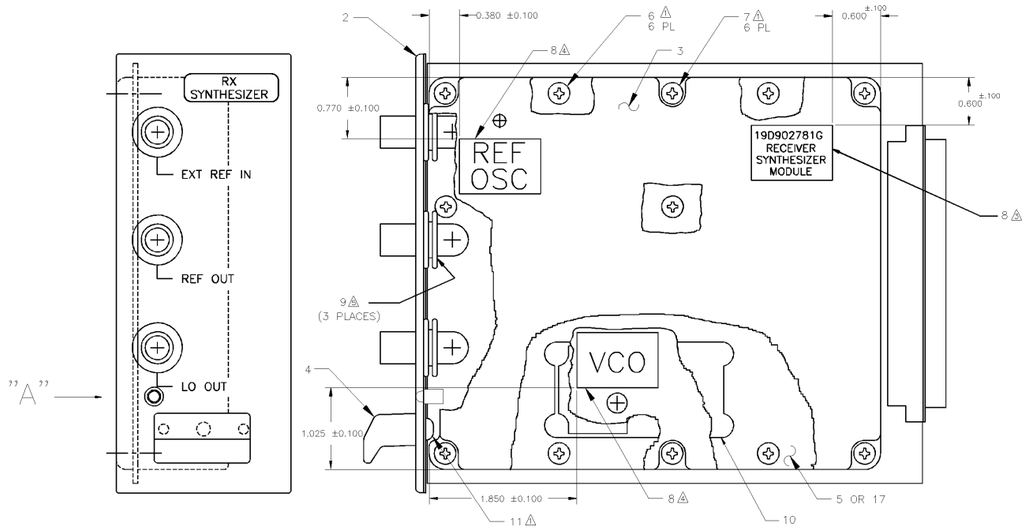
TROUBLESHOOTING CHART

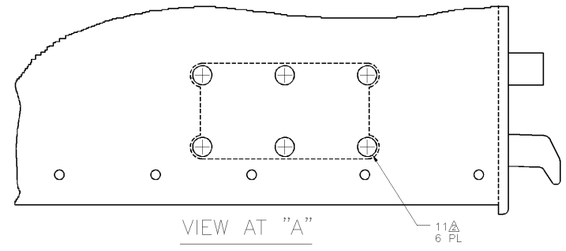
SYMPTOM	AREAS TO CHECK	INDICATIONS
I. Loop Fails To Lock	1. Check for: +8 Vdc at U16-3, +5 Vdc at U15-3 +8 Vdc at Q8-C.	Bad Regulation circuitry. Troubleshoot using standard procedures.
	2. Check for 12.8 MHz reference at U6-2, and U6-3. Typical Levels: 500 mVpp @ U6-2 2.5 Vpp @ U6-3	Reference Osc. Module defective or supply not present or low. Proceed to reference oscillator section II.
	3. Check for LO output @ J2. F_{LO} ±5 MHz,0dBm nominal.	LO tuning incorrect, or buffer amplifier bad. Proceed to LO tuning and power section III.
	4. Check Prescaler output @ U5-4. Typically: 2-4 MHz square wave @ 1.25 Vpp.	If LO power is good, Check for 3.2 Vdc @ U2-3. Replace U2, then U5 if necessary.
	5. Check for CLOCK, DATA, and ENABLE signals are reaching U6 pins 11,12, and 13 respectively. (0, 8V logic levels)	Bad digital control circuitry. Troubleshoot using standard procedures. Ensure all programming signals are present at J1. (CLOCK,DATA,ENABLE,A0,A1 and A2)
	6. Check Ramp Signal @ U6-15. It should be 5 kHz nominal.	If reference oscillator and programming signals are present for proper programming information. Last resort - replace Synthesizer IC U6.
II. Reference OSC. not present or low power.	1. Check for 4.3 Vdc supply at junction of R5 and C41.	Bad supply switch Q2 or wrong Control Signal Internal Osc. Troubleshoot using standard procedures. Replace Y1 as last resort
	2. Check 12.8 MHz signal @ Q13-E. Should be approx. 350 mVpp.	Bad buffer amplifier Q13. Troubleshoot using standard procedures.

Continued

TROUBLESHOOTING CHART (Continued)

SYMPTOM	AREAS TO CHECK	INDICATIONS
III. LO power low or tuned out of band.	1. Check tuning with 6 Vdc applied using test procedure. F_{LO}±5 MHz	LO tuning incorrect. Retune following test procedure.
	2. Check DC bias at Buffer Amplifiers U1, U2, & U3 pin 3 Typ. 3.2 Vdc.	Bad Buffer Amplifier. Replace bad part.
IV. LO signal not present. (i.e. Q1 does not oscillate)	1. Check DC bias at Q1 drain. (Typ. +8Vdc)	Replace Q1.
	2. Check DC bias at Q1 source. (Typ. +0.9 Vdc)	

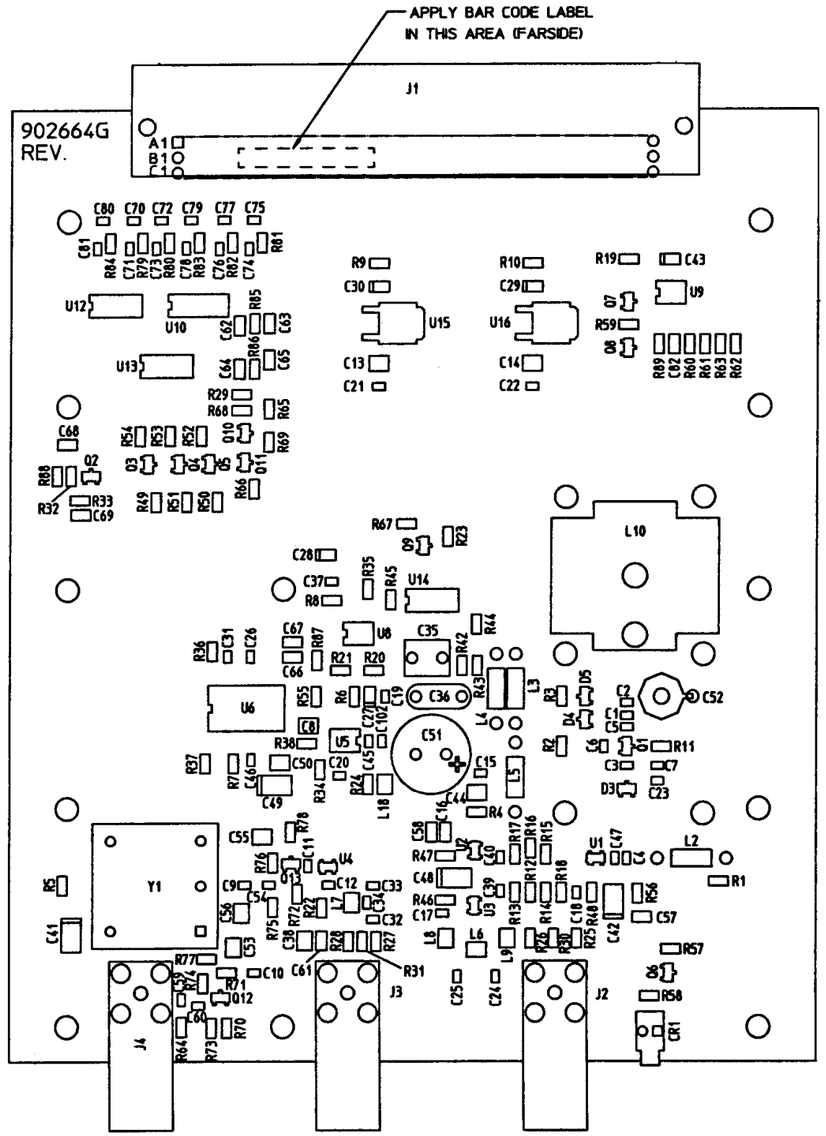




NOTES:
1. TORQUE SCREWS, ITEMS 6 AND 7, TO 10.0 ±1.3 INCH POUNDS.
2. TORQUE SCREWS, ITEM 11 , TO 20 ± 1.3 INCH POUNDS.
3. MARK AS SHOWN WITH APPLICABLE GROUP NUMBER PER 19A115740P1.
4. MARK AS SHOWN PER 19A115740P1
5. FORM ITEM 9 AROUND BNC CONNECTOR BEFORE ASSEMBLY OF COMPONENT BOARD (ITEM 5 OR 17) WITH ITEM 2

RECEIVER SYNTHESIZER MODULE 19D902781G1 & G2

(19D902781, Sh1, Rev. 7)



LEAD IDENTIFICATION FOR
Q1-Q8
(SOT) TRANSISTORS
(TOP VIEW)

(B) 2
3 (C)
(E) 1

LEAD IDENTIFICATION FOR
U1-U4
(SOT) INT CKT
(TOP VIEW)

OUTPUT
GND
GND
INPUT

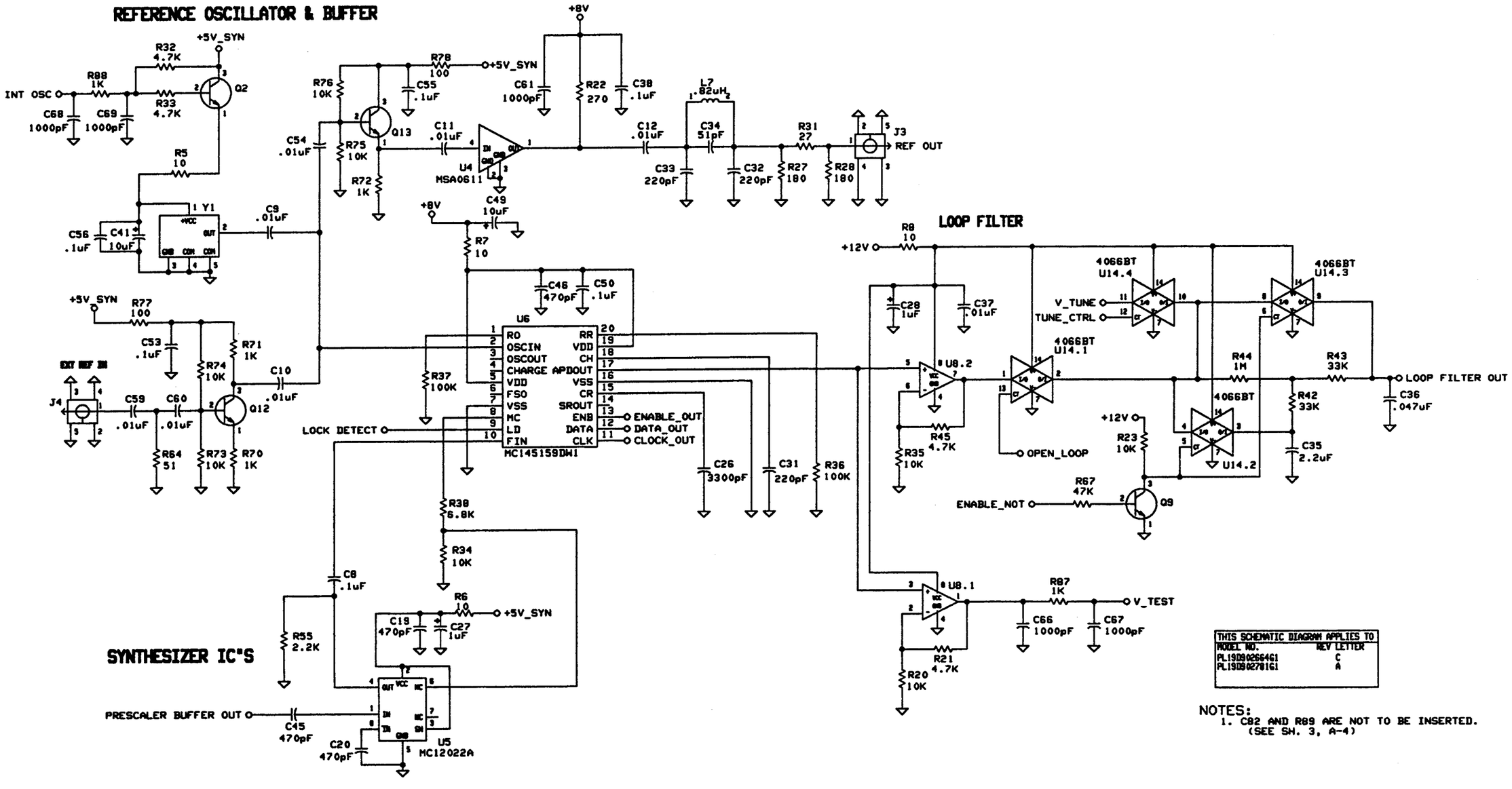
LEAD IDENTIFICATION FOR
D3-D5
(SOT) DIODES
(TOP VIEW)

2
3
1

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

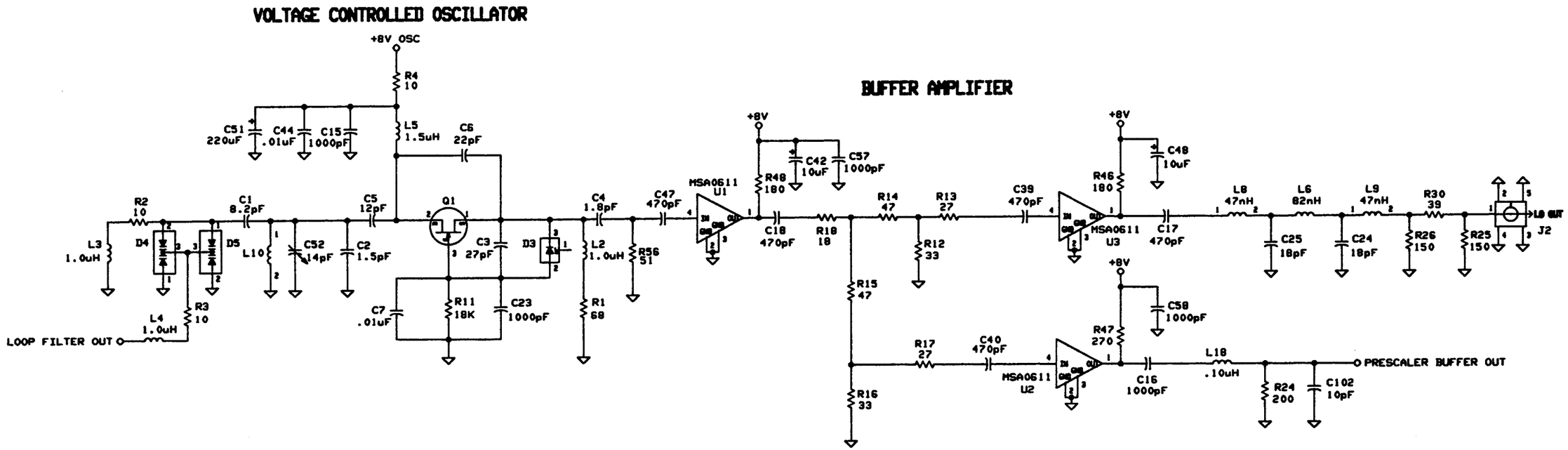
RECEIVER SYNTHESIZER BOARD
19D902664G1 & G2

(19D902664, Sh. 1, Rev. 10)



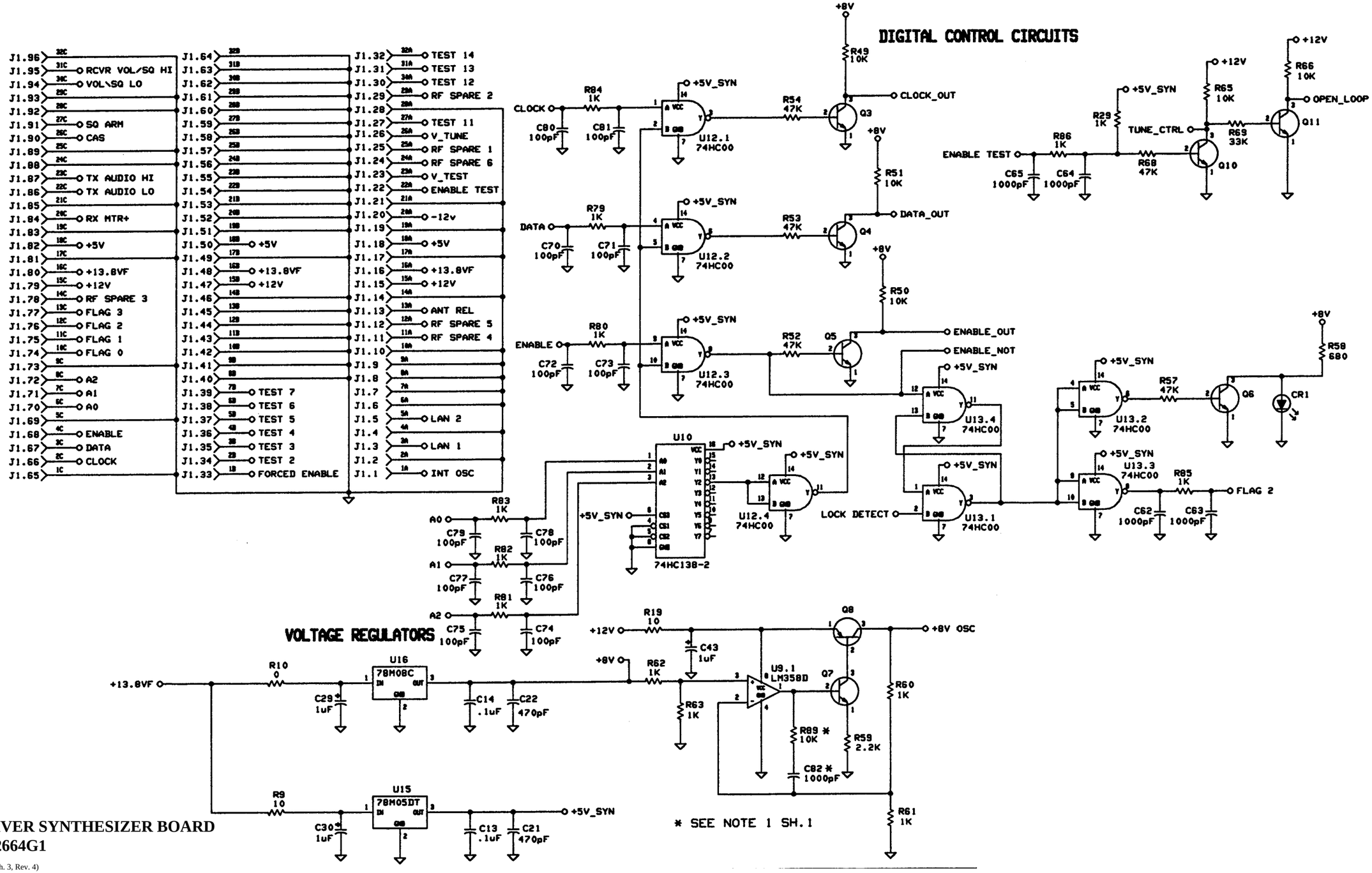
RECEIVER SYNTHESIZER BOARD
19D902664G1

(19D903621, Sh. 1, Rev. 4)



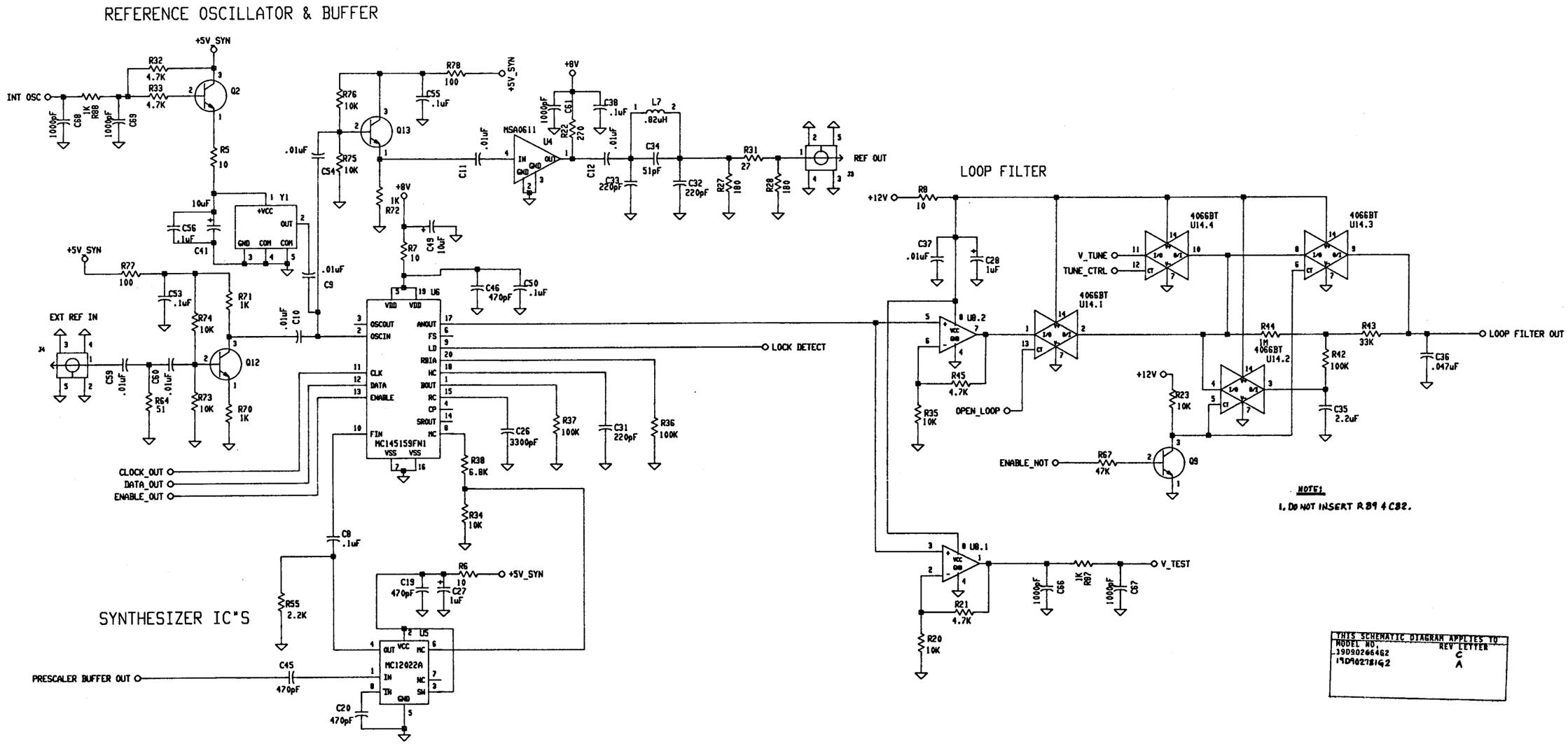
RECEIVER SYNTHESIZER BOARD
19D902664G1

(19D903621, Sh. 2, Rev. 4)



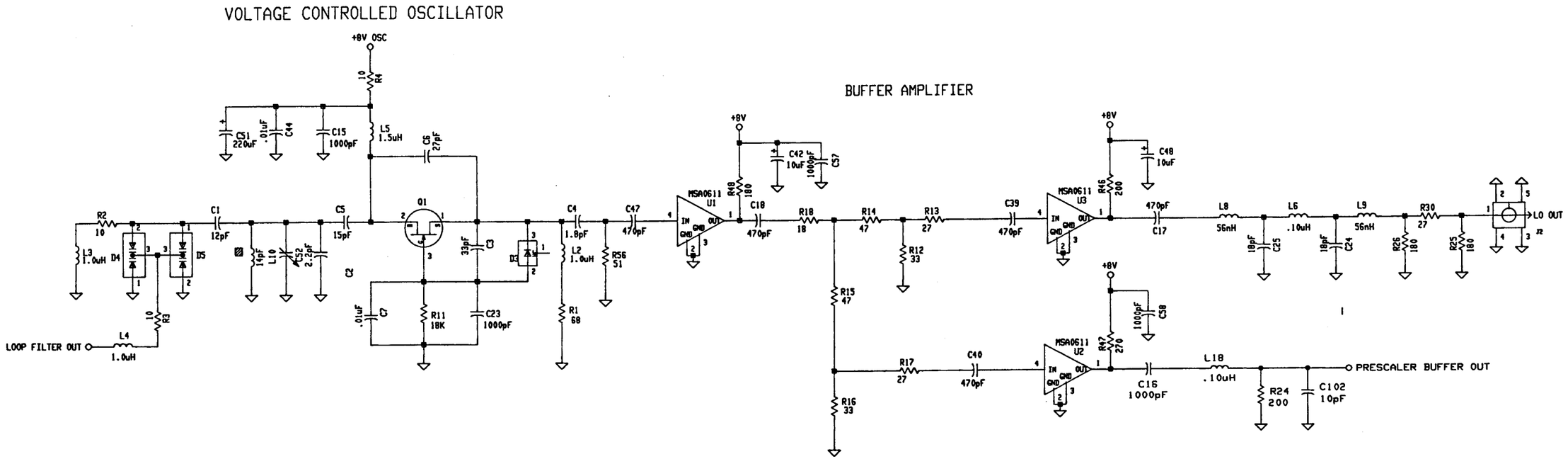
RECEIVER SYNTHESIZER BOARD
19D902664G1

(19D903621, Sh. 3, Rev. 4)



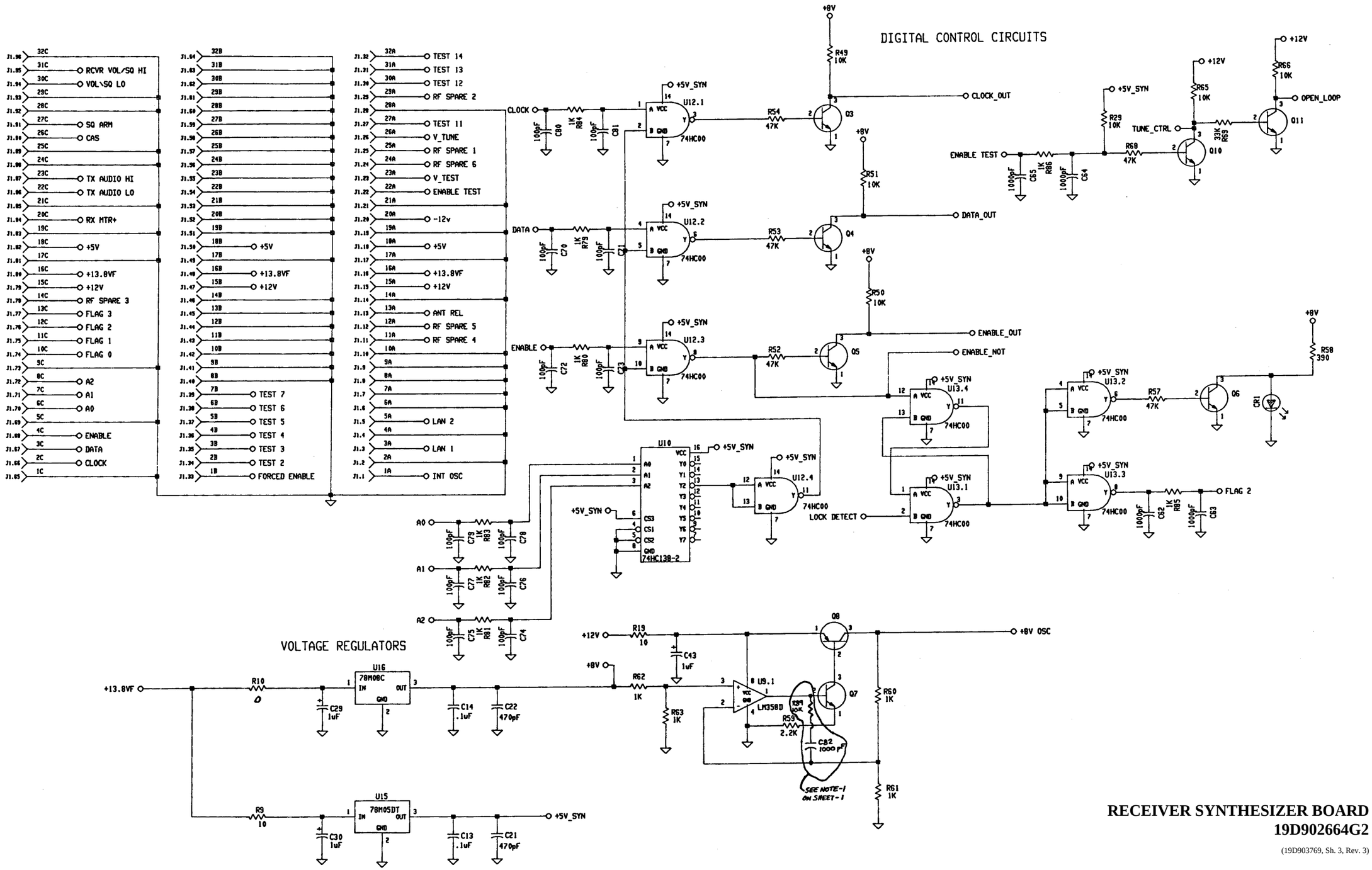
RECEIVER SYNTHESIZER BOARD
19D902664G2

(19D903769, Sh. 1, Rev. 3)



RECEIVER SYNTHESIZER BOARD
19D902664G2

(19D903769, Sh. 2, Rev. 3)



RECEIVER SYNTHESIZER BOARD
19D902664G2

(19D903769, Sh. 3, Rev. 3)

RECEIVER SYNTHESIZER MODULE
19D902781G1-G2
ISSUE 4

SYMBOL	PART N0.	DESCRIPTION
		——— MISCELLANEOUS ——
2	19D902508P3	Chassis.
3	19D902509P3	Cover.
4	19D902555P1	Handle.
5	19D902664G1	Receiver Synthesizer Board, (Used in G1).
6	19A702381P506	Screw, thread forming: TORX, No. M3.5 - 0.6 X 6.
7	19A702381P513	Screw, thread forming: TORX, No. M3.5 - 0.6 X 13.
9	19B802690P1	RF Shielding Grommet.
10	19D902824P1	RF Casting.
11	19A702381P508	Screw, thd. form: No. 3.5-0.6 x 8. (Used in G1, G2, G1 and G2).
17	19D902664G2	Receiver Synthesizer Board. (Used in G2).
		RECEIVER SYNTHESIZER BOARD 19D902664G1 - G2
		———— CAPACITORS ———
C1	19A702236P28	Ceramic: 12 pF ±5%, 50 VDCW, temp coef 0±30 PPM. (Used in G2).
C1	19A702236P23	Ceramic: 8.2 pF ±.25 pF, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C2	19A702236P10	Ceramic: 2.2 pF ±2.5 pF, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G2).
C2	19A702236P8	Ceramic: 1.5 pF ±.25 pF, 50 VDCW. (Used in G1).
C3	19A702236P38	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G2).
C3	19A702236P36	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G1).
C4	19A702236P9	Ceramic: 1.8 pF ±0.25 pF, 50 VDCW, temp coef 0 ±30 PPM.
C5	19A702236P30	Ceramic: 15 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G2).
C5	19A702236P28	Ceramic: 12 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C6	19A702236P36	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G2).
C6	19A702236P34	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C7	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C8	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C9 thru C12	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C13 and C14	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C15	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C16 thru C22	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef. 0 ±30 PPM/ºC.
C23	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C24 and C25	19A702236P32	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM
C26	19A702052P8	Ceramic: 3300 pF ±10%, 50 VDCW.
C27 thru C30	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C31 thru C33	19A702052P1	Ceramic: 220 pF ±10%, 50 VDCW.
C34	19A702236P43	Ceramic: 51 pF ±5, 50 VDCW, ±30 PPM/°C.
C35	19A703684P3	Metallized polyester: 2.2 µF ±10%, 50 VDCW.
C36	19A703902P3	Metal: 0.047 µF ±10%, 50 VDCW.
C37	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C38	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C39 and C40	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C41 and C42	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C43	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C44	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C45 thru C47	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C48 and C49	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C50	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C51	19A701225P3	Electrolytic: 220 µF, -10+50%, 25 VDCW.
C52	19A134227P5	Variable: 1.5 to 14 pF, 100 VDCW.
C53	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C54	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C55 and C56	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C57 and C58	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C59 and C60	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C61 thru C69	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C70 thru C81	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C102	19A702236P25	Ceramic: 10 pF ±25pF, 50 VDCW, temp coef. 0 ±30 PPM/ºC.
		———— DIODES ————
CR1	19A703595P10	Diode, Optoelectric: Red; sim to HP HLMP-1301-010.
D3	19A705377P1	Silicon, Hot Carrier: sim to MMB0201.
D4 and D5	19A149674P1	Silicon, capacitive: sim to Toko KV1410.
J1	19B801587P7	Connector, DIN: 96 male contacts, right angle mounting; sim to AMP 650887-1.
J2 thru J4	19A115938P24	Connector, receptacle.
		———— INDUCTORS ———
L2 thru L4	19A700024P13	Coil, RF: 1.0 µH ±10%.
L5	19A700024P15	Coil, RF: 1.5 µH ±10%.
L6	19A705470P13	Coil: 0.10 µH ±20%. (Used in G2).
L6	19A705470P12	Coil, fixed. (Used in G1).
L7	19A705470P24	Coil, fixed: 1.5 µH ±10%.
L8	19A705470P10	Coil, fixed: 56 nH ±20%. (Used in G2).
L8	19A705470P9	Coil, Fixed: 47 nH; sim to Toko 380NB-47nM. (Used in G1).
L9	19A705470P10	Coil, fixed: 56 nH ±20%. (Used in G2).
L9	19A705470P9	Coil, Fixed: 47 nH; sim to Toko 380NB-47nM. (Used in G1).
L10	19C851001P3	Coil, RF: sim to Paul Smith SK-901-1. (Used in G2).
L10	19C851001P1	Coil, RF: sim to Paul Smith SK901-1. (Used in G1).
L18	19A705470P13	Coil: 0.10 µH ±20%
		——— TRANSISTORS ———
Q1	19A702524P2	N-Type, field effect; sim to MMBFU310.
Q2 thru Q7	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q8	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q9 thru Q13	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		———— RESISTORS———
R1	19B800607P680	Metal film: 68 ohms ±5%, 1/8 w.
R2 thru R9	19B800607P100	Metal film: 10 ohms ±5%, 1/8 w.
*R10	19B800607P1	Metal film: 0 ohms.
R11	19B800607P183	Metal film: 18K ohms ±5%, 1/8 w.
R12	19B800607P330	Metal film: 33 ohms ±5%, 1/8 w.
R13	19B800607P270	Metal film: 27 ohms ±5%, 1/8 w.
R14 and R15	19B800607P470	Metal film: 47 ohms ±5%, 1/8 w.
R16	19B800607P330	Metal film: 33 ohms ±5%, 1/8 w.
R17	19B800607P270	Metal film: 27 ohms ±5%, 1/8 w.
R18	19B800607P180	Metal film: 18 ohms ±5%, 1/8 w.
R19	19B800607P100	Metal film: 10 ohms ±5%, 1/8 w.
R20	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R21	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R22	19B800607P271	Metal film: 270 ohms ±5%, 1/8 w.
R23	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R24	19B800607P201	Metal film: 200 ohms ±5%, 1/8 w.
R25	19B800607P151	Metal film: 150 ohms ±5%, 1/8 w. (Used in G1).
R26	19B800607P181	Metal film: 180 ohms ±5%, 1/8 w. (Used in G2).
R26	19B800607P151	Metal film: 150 ohms ±5%, 1/8 w. (Used in G1).
R27 and R28	19B800607P181	Metal film: 180 ohms ±5%, 1/8 w.
R29	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R30	19B800607P270	Metal film: 27 ohms ±5%, 1/8 w. (Used in G2).
R30	19B800607P390	Metal film: 39 ohms ±5%, 1/8 w. (Used in G1).
R31	19B800607P270	Metal film: 27 ohms ±5%, 1/8 w.
R32 and R33	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R34 and R35	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R36 and R37	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R38	19B800607P682	Metal film: 6.8K ohms ±5%, 1/8 w.
R42	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w. (Used in G2).
R42	19B800607P333	Metal film: 33K ohms ±5%, 1/8 w. (Used in G1).
R43	19B800607P333	Metal film: 33K ohms ±5%, 1/8 w.
R44	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R45	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R46	19B800607P201	Metal film: 200 ohms ±5%, 1/8 w. (Used in G2).
R46	19B800607P181 (Used in G1).	Metal film: 180 ohms ±5%, 1/8 w.
R47	19B800607P271	Metal film: 270 ohms ±5%, 1/8 w.
R48	19B800607P181	Metal film: 180 ohms ±5%, 1/8 w.
R49 thru R51	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R52 thru R54	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R55	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 w.
R56	19B800607P510	Metal film: 51 ohms ±5%, 1/8 w.
R57	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R58	19B800607P681	Metal film: 680 ohms ±5%, 1/8 w.
R59	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 w.
R60 thru R63	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R64	19B800607P510	Metal film: 51 ohms ±5%, 1/8 w.
R65 and R66	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R67 and R68	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.

*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R70 thru R72	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R73 thru R76	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R77 and R78	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R79 thru R88	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
		—— INTEGRATED CIRCUITS ——
U1 thru U4	19A705927P1	Silicon, bipolar: sim to Avantek MSA-0611.
U5	19A149944P201	Dual Modulus Prescaler: sim to MC12022A.
U6	19B800902P5	Synthesizer, custom: CMOS, serial input.
U8 and U9	19A702293P3	Linear: Dual Op Amp; sim to LM358D.
U10	19A703471P320	Digital: 3-Line To 8-Line Decoder; sim to 74HC138.
U12 and U13	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U14	19A702705P4	Digital: Quad Analog Switch/ Multiplexer; sim to 4066BM.
U15	19A704971P8	Voltage Regulator, Positive: sim to Motorola MC78M05CDT.
U16	19A704971P10	Voltage Regulator, Positive: sim to Motorola MC78M08CDT.
		———— CRYSTALS ———
Y1	19B801351P12	Crystal Oscillator; 14.850 MHz, temperature compensated.

PRODUCTION CHANGES

Changes in the equipment to improve or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2

To improve regulator operation at low supply voltage. Changed resistor R10. Resistor R10 was 10 ohms (19B800607P100).

REV. B - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2

To accommodate SOG synthesizer IC package U6 (PLCC package discontinued) and make provision for RC compensation network (R89, C82) in 10-Volt regulator circuit. Resistor R89 and capacitor C82 are not installed. Modified printed wire board layout (Printed wire board changed from 19D902665P1R1 to 19D902665P1R2). Changed U6. Synthesizer U6 was 19B800902P5.

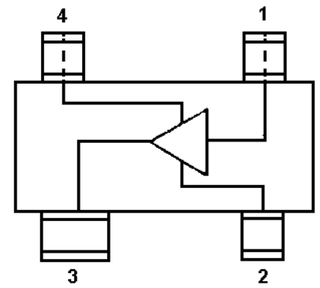
REV. A - RECEIVER SYNTHESIZER MODULE 19D902781G1 & G2

To install RF shielding grommets. Installed item 9 RF shielding grommets (19B705470P1) on three BNC connectors of input/output RF ports.

REV. C - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2

To add filtering in the output circuit of the pre-scaler buffer amplifier. Changed capacitor C16. Capacitor C16 was 19A702052P3 (*470 pF*). Added capacitor C102 and inductor L18. Changed resistor R24. Resistor R24 was 19B800607P510 (*51 Ohms*).

U1 thru U4
19A705927P1
Silicon Bipolar IC



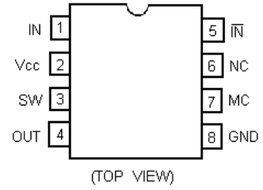
PIN 1. RF INPUT
2. GROUND
3. RF OUTPUT AND BIAS
4. GROUND

U5
19A149944P201
Modulus Prescaler

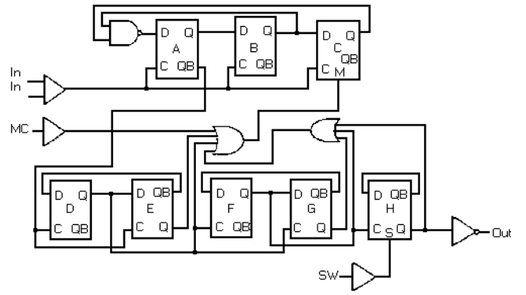
FUNCTION TABLE		
SW	MC	DIVIDE RATIO
H	H	64
H	L	65
L	H	128
L	L	129

SW: H = Vcc L = OPEN
MC: H = 2.0V TO Vcc
L = GND TO 0.8V

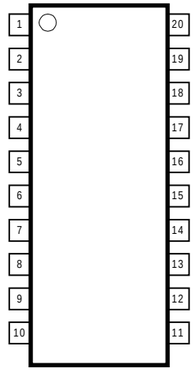
PIN ASSIGNMENT

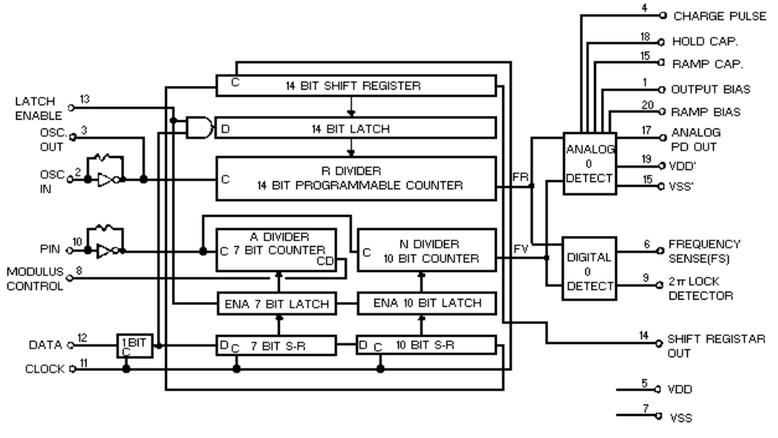


(TOP VIEW)

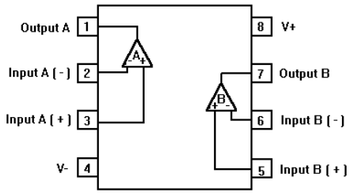


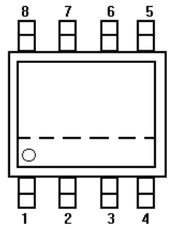
U6
19B800902P7
Synthesizer



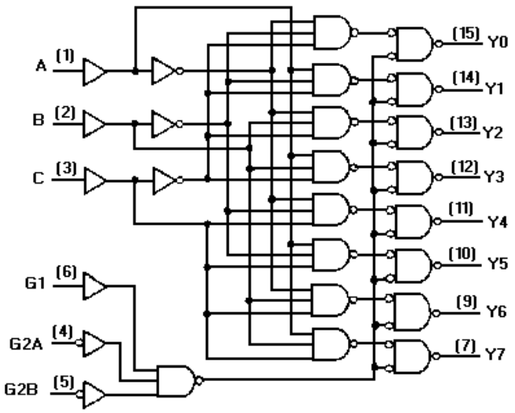


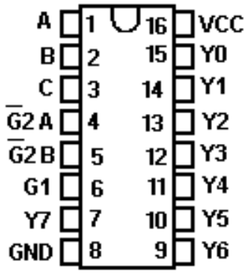
U8 & U9
19A702293P2
Dual Operational Amplifier



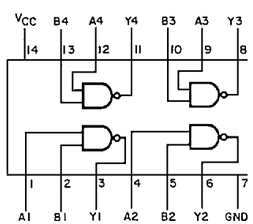


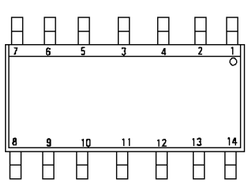
U10
19A703471P120
Decoder/Demux





U12 & U13
19A703483P302
Logic Gate/Inverter

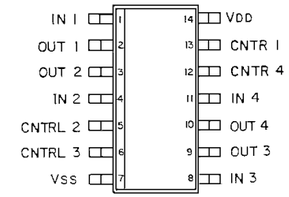




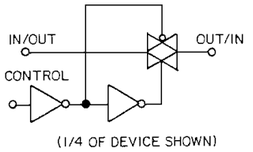
U14
19A702705P4
Quad Analog Switch

QUAD ANALOG SWITCH/MULTIPLEXER
19A702705P1,P4
(CMOS)

PIN CONFIGURATION



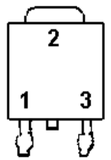
LOGIC DIAGRAM



(1/4 OF DEVICE SHOWN)

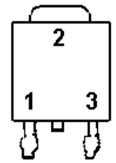
CONTROL	SWITCH
0	OFF
1	ON

U15
19A704971P8
+5 Regulator



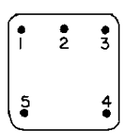
PIN	FUNCTION
1	INPUT
2	GROUND
3	OUTPUT

U16
19A70497P10
+8V Regulator



PIN	FUNCTION
1	INPUT
2	GROUND
3	OUTPUT

Y1
19B801351P12
Crystal Oscillator



PIN CONNECTIONS

1. +Vcc
2. OUTPUT
3. COMMON & CASE
4. COMMON & CASE *
5. COMMON & CASE

* PIN 4 IS PERMISSIBLE BUT NOT NECESSARY FOR OPERATION.

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